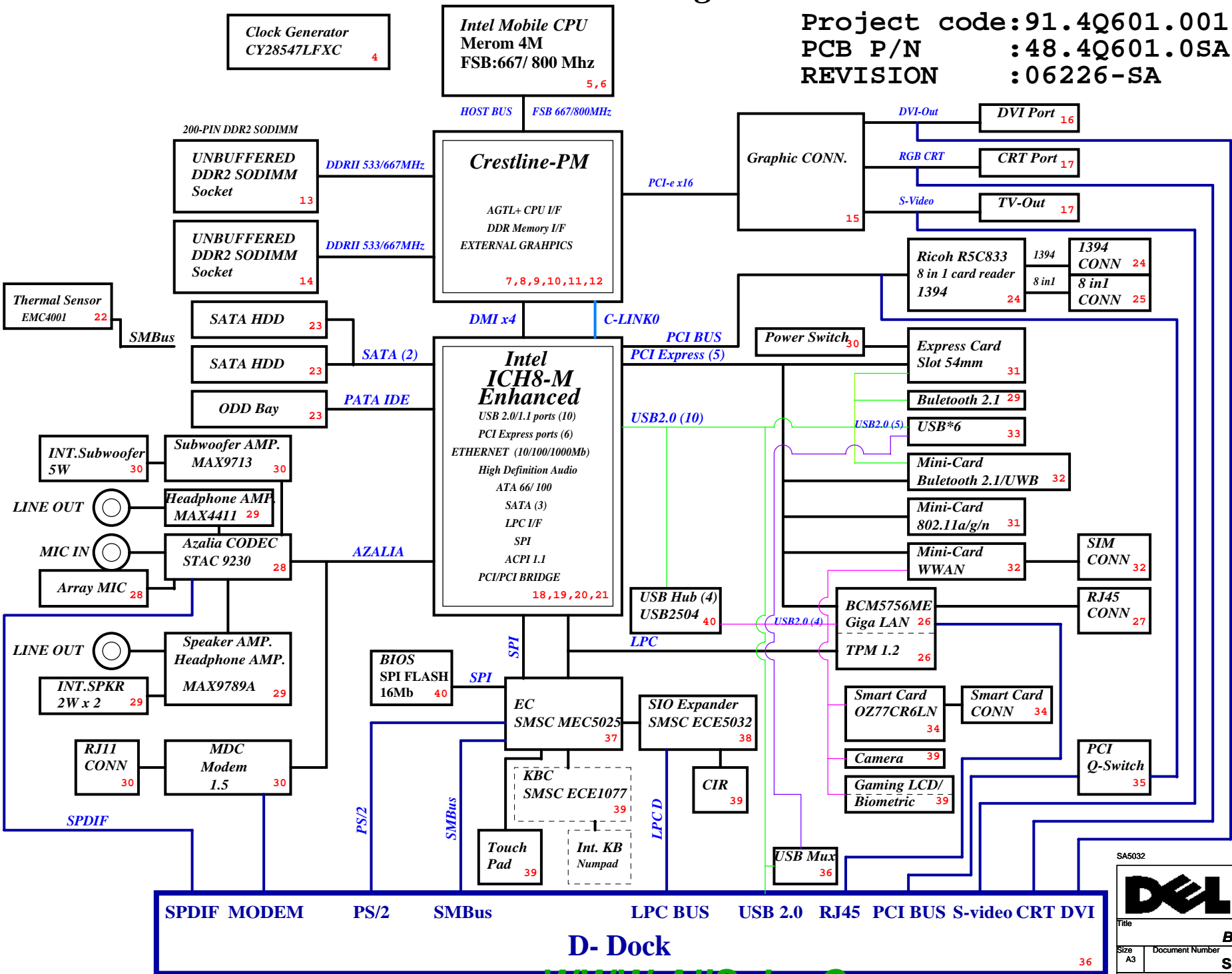


Siberia / Converse Block Diagram

Project code: 91.4Q601.001
PCB P/N : 48.4Q601.0SA
REVISION : 06226-SA



System DC/DC	
TPS51120 50	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO
System DC/DC	
SN0508073 48	
+PWR_SRC	+1.05V_VCCP +1.5V_RUN
DDR2 DC/DC	
SN0508073 49	
+PWR_SRC	+1.8V_SUS +1.25V_RUN
LDO	
TPS51100 51	
+1.8V_SUS	+0.9V_DDR_VTT
LDO	
MAX668 51	
+PWR_SRC	+12V_S

Battery Charger	
ISL88731 45	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC	
ISL6260C 46,47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER	
L1: TOP	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Signal	
L7: GND	
L8: BOT	

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Title

Size A3 Document Number

Date: Friday, September 01, 2006 Sheet 1 of 53

Rev SA

BLOCK DIAGRAM

Siberia / Converse

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CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15

IO_VOUT[2,1,0]

Bit2	Bit1	Bit0	IO_VOUT[2,1,0]
IO_VOUT2	IO_VOUT1	IO_VOUT0	
0	0	1	0.3V
0	0	0	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Lane Reserved
CFG 20	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
HL(0)	XOR Mode Enabled
HL(1)	All Z Mode Enabled
HL(1)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	No use
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
Dock	AD24	A	0	0
1394/ MediaCard	AD17	C	1	1

USB TABLE

ICH

USB0	Ext Side (Left)
USB1	Ext Side (Right)
USB2	Ext I/O BD Side (Top)
USB3	Ext I/O BD Side (Bottom)
USB4	Ext Back (Bottom)
USB5	Dock/Ext Back (Top)
USB6	Express Card
USB7	BT
USB8	3rd mini card
USB9	USB Hub

USB Hub

USB1	SmartCard
USB2	Gaming LCD/Biometric
USB3	Camera
USB4	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RST#p3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(Default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

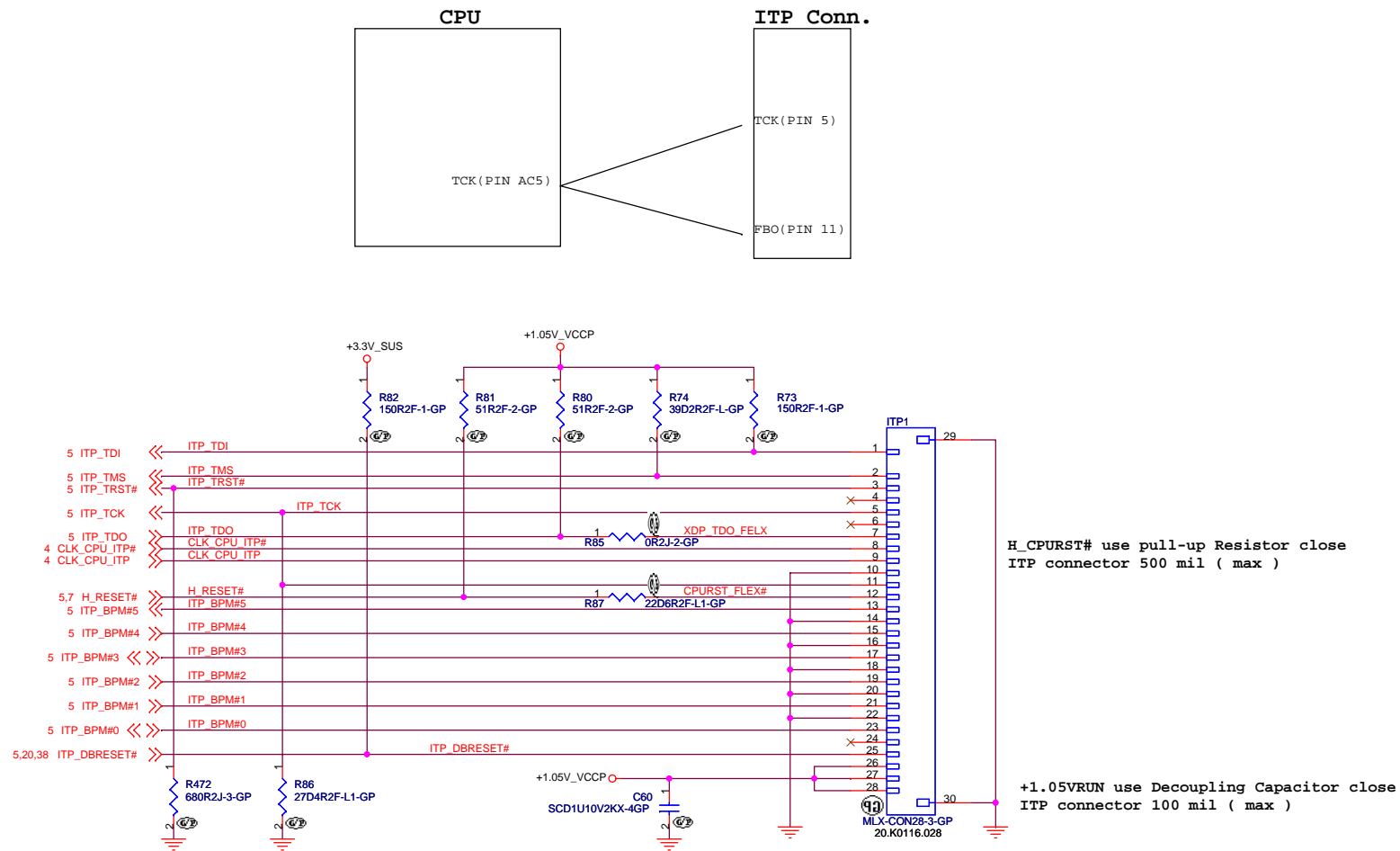
INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K



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Title		
Table of Content		
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Siberia / Converse		
Date: Friday, September 01, 2006	Sheet 2	of 53

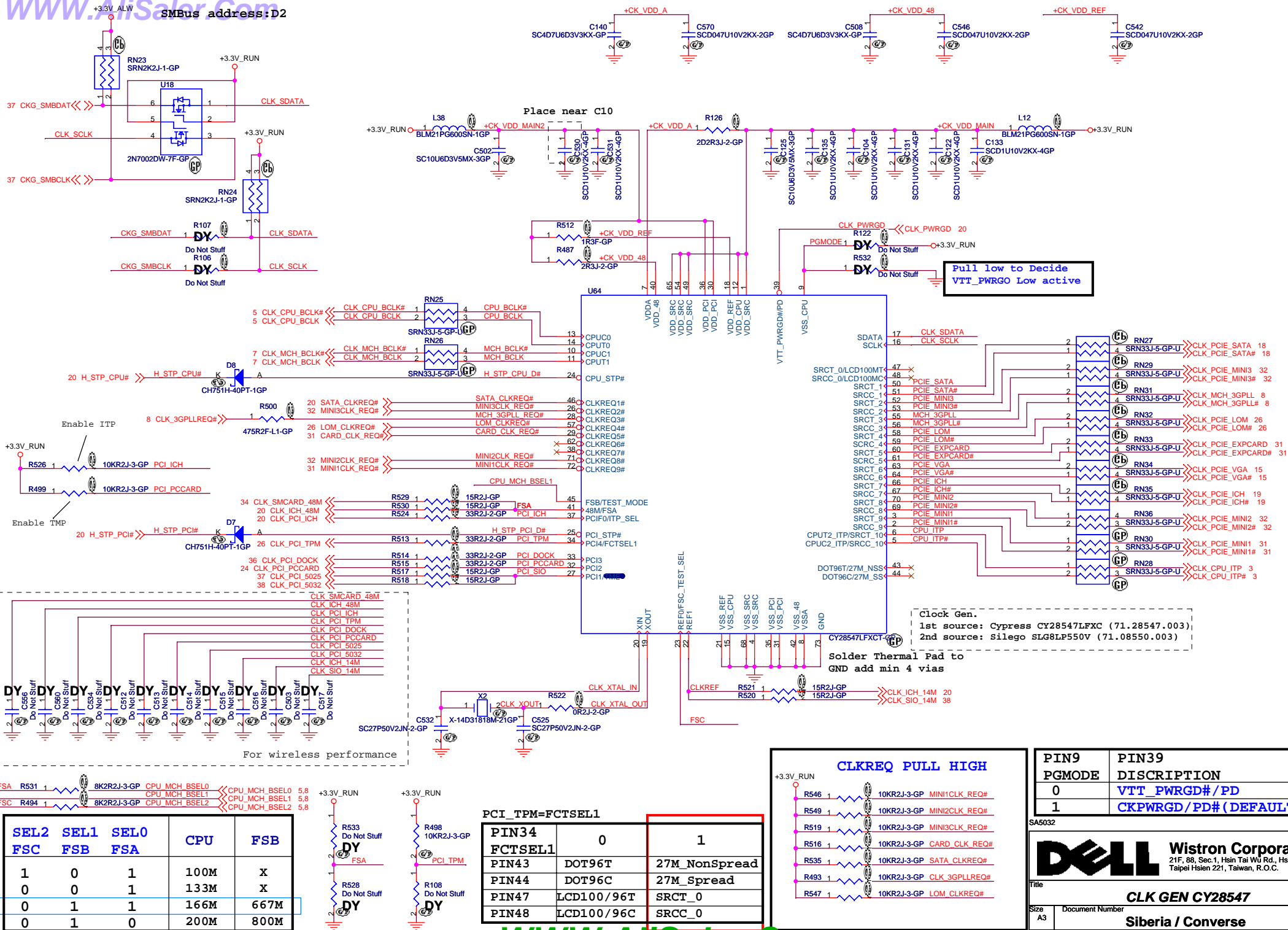


ITP Debug Conn.

SA5032



Title				
ITP Debug				
Size	Document Number			Rev
A3	Siberia / Converse			SA
Date:	Friday, September 01, 2006	Sheet	3 of	53

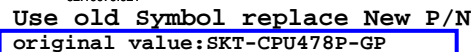


PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD# / PD
1	CKPWRGD / PD# (DEFAULT)

SA5032

Title
CLK GEN CY28547

Size A3	Document Number Siberia / Converse	Rev SA
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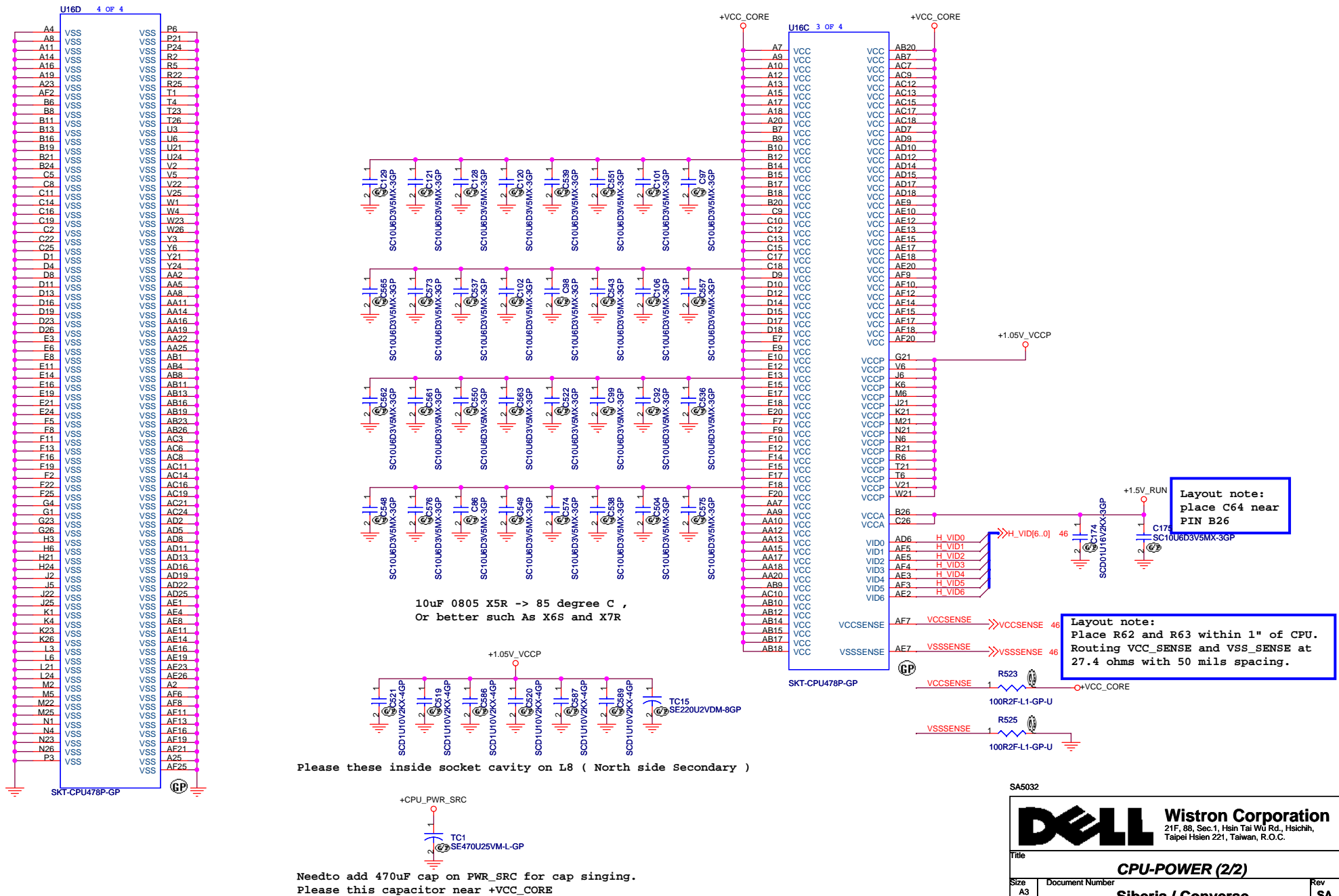
Do Not STOP69 TEST3
Do Not STOP58 TEST5

For the purpose of testability, route these signals through a ground referenced Zo=55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Make COMP[3..0] traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

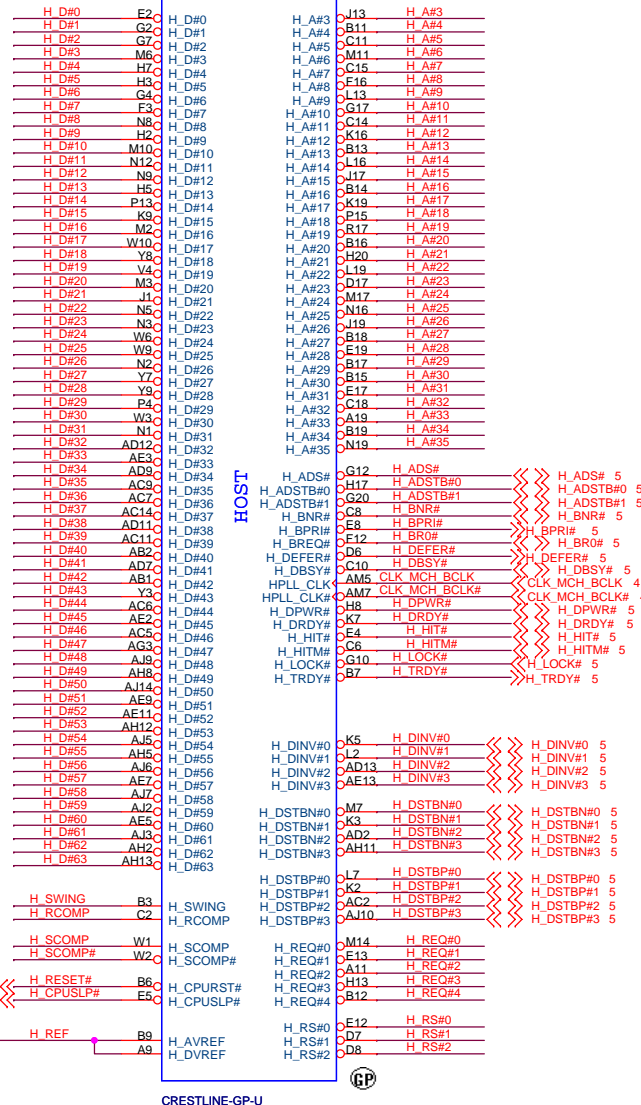
COMP 0,2 connect $Z_0=27.4\text{ohm}$.

COMP 1,3 connect $Z_0=55\text{ohm}$.

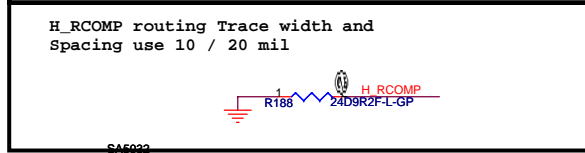
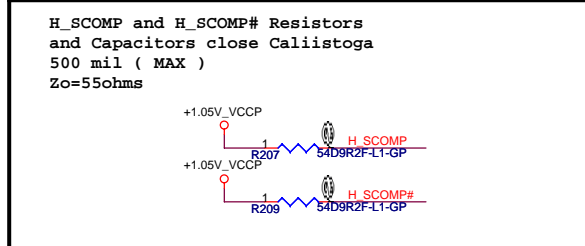
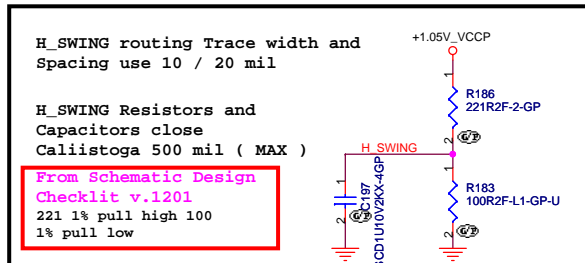
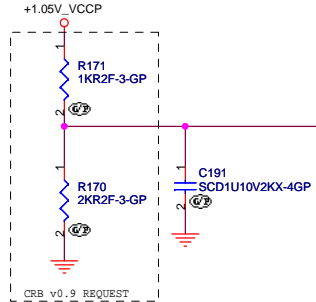


H_D#[63..0] <<>> H_D#[63..0] 5
H_A#[35..3] <<>> H_A#[35..3] 5
H_REQ#[4..0] <<>> H_REQ#[4..0] 5
H_RS#[2..0] >>> H_RS#[2..0] 5

U34A 1 OF 10



H_REF Decoupling Crestline
close Crestline 100 mil

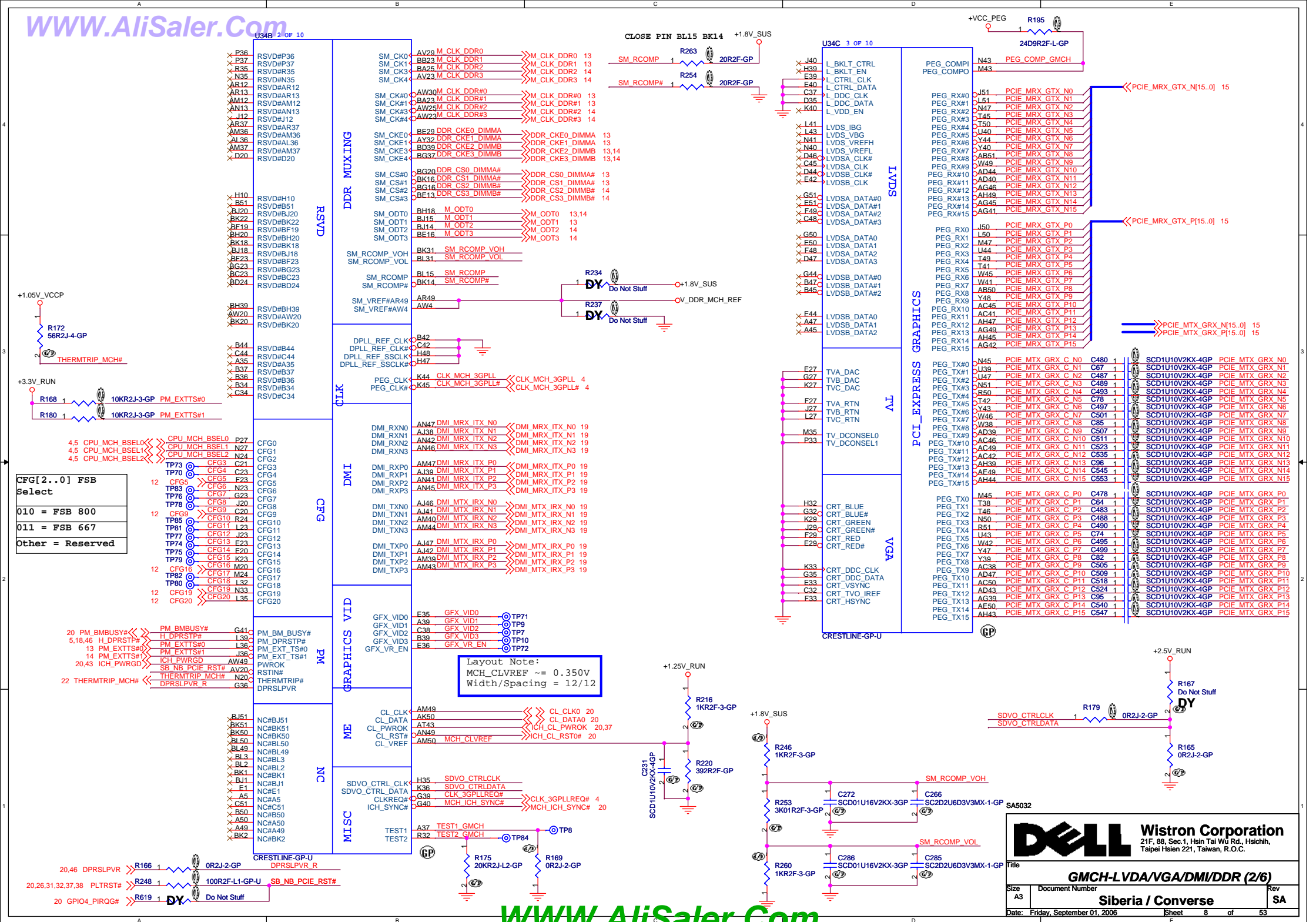


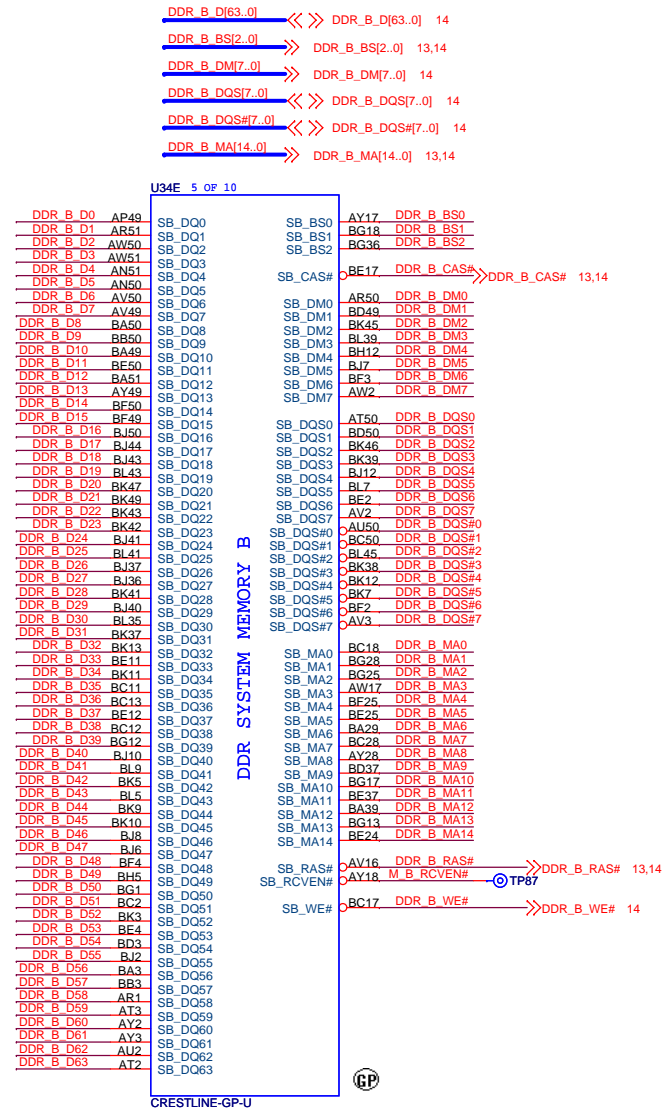
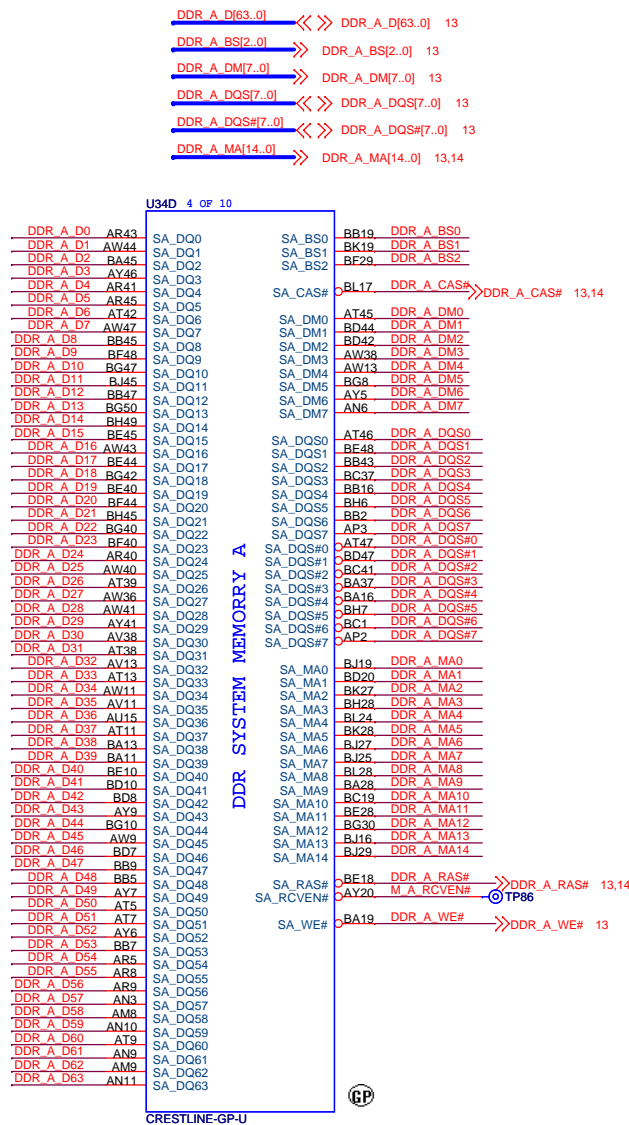
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Title: **GMCH-FSB LIBC (1/6)**

Size A3 Document Number **Siberia / Converse** Rev SA

Date: Friday, September 01, 2006 Sheet 7 of 53

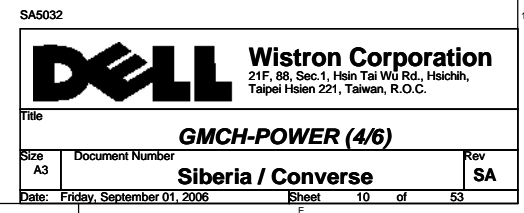




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Title			GMCH-DDR (3/6)	
Size	Document Number	Siberia / Converse		Rev
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Date:	Friday, September 01, 2006	Sheet	9	of 53



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Title

GMCH-POWER/FILTERR (5/6)

Size

Document Number	
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Siberia / Converse

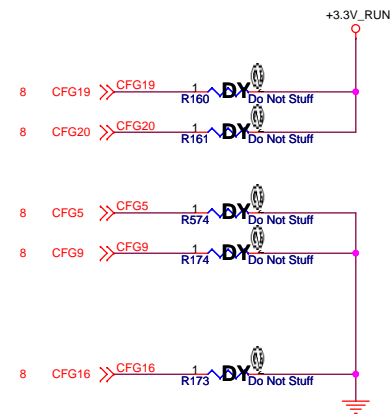
Rev

Date: Friday, September 01, 2006

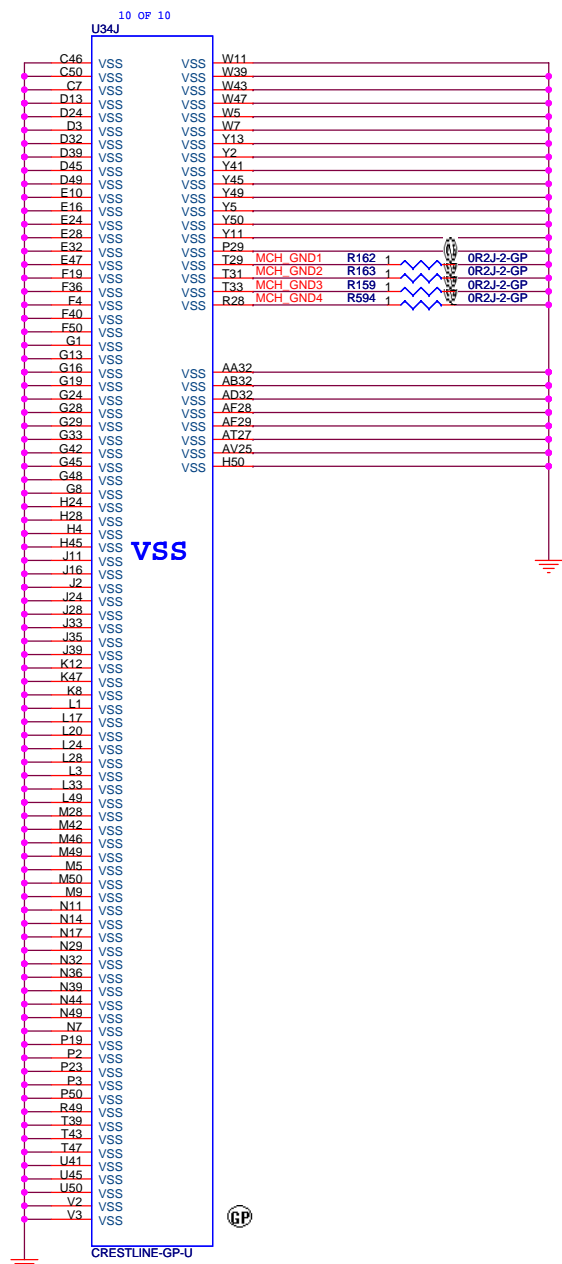
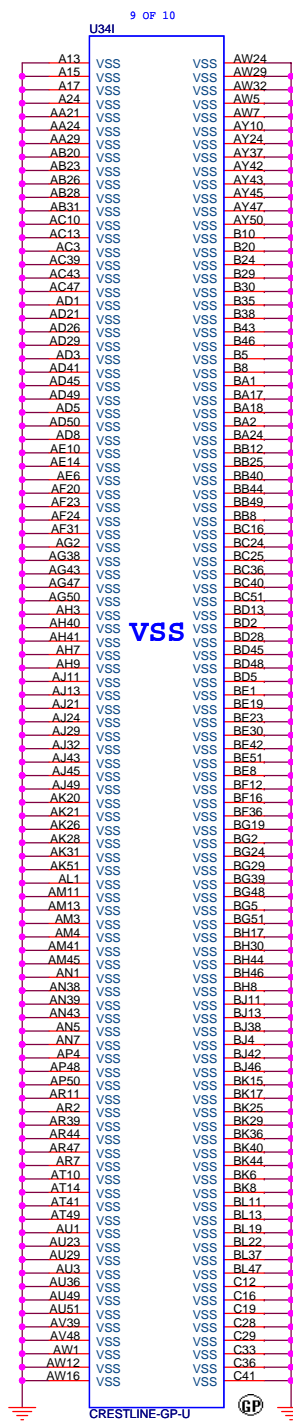
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3

Layout Note:
Location of all MCH CFG strap resistors need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode (Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 18 VCC select	1.05V	1.5V
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous
CFG 12 CFG 13	XOR/ALL-Z	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	



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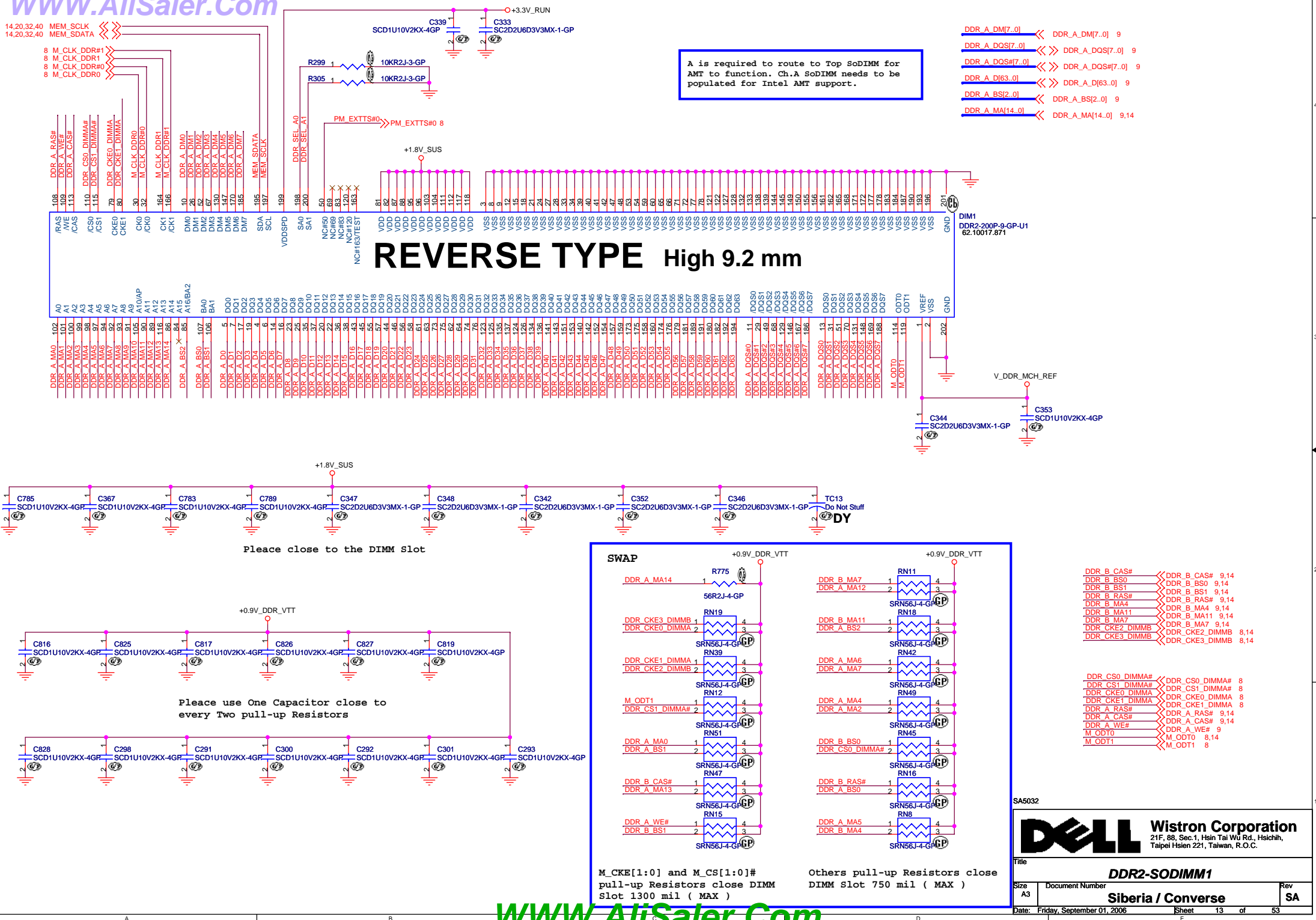
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH-GND (6/6)**

Size A3 Document Number: **Siberia / Converse** Rev: **SA**

Date: Friday, September 01, 2006 Sheet 12 of 53

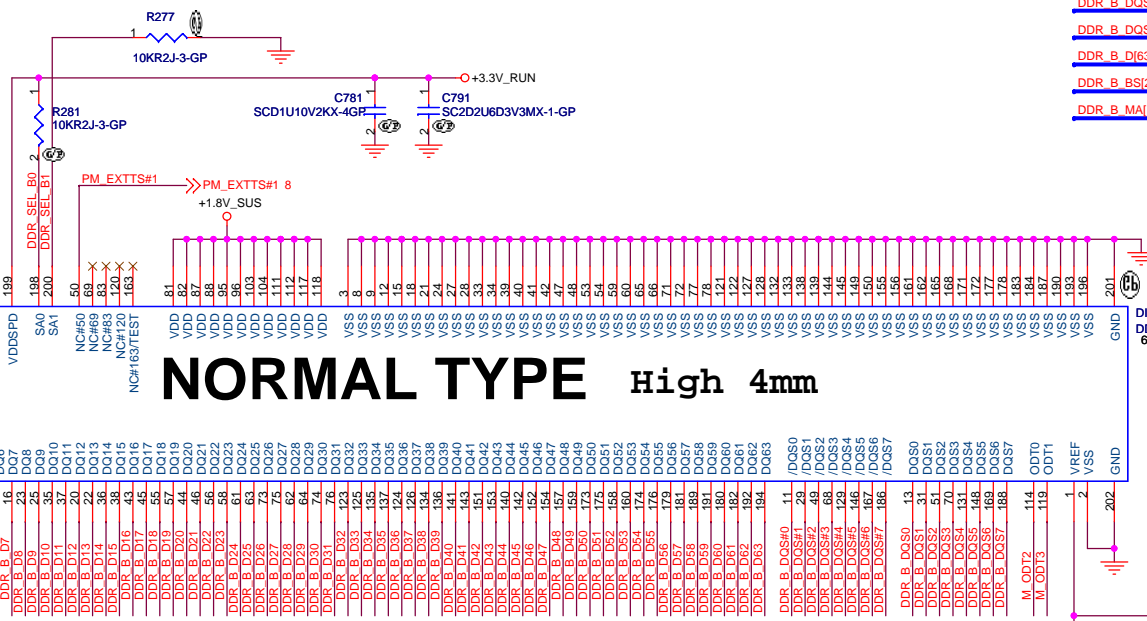
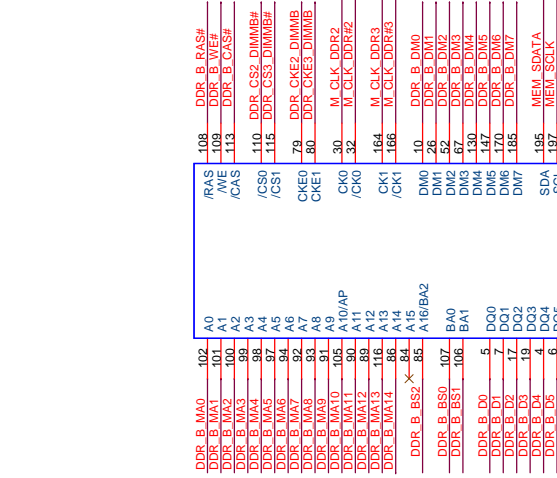
14,20,32,40	MEM_SCLK	↔
14,20,32,40	MEM_SDATA	↔



M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2

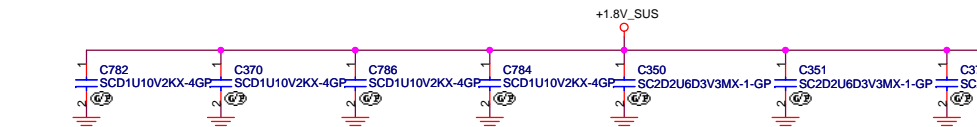
13,20,32,40 MEM_SCLK
13,20,32,40 MEM_SDAT4

8 M_CLK_DDR#2
8 M_CLK_DDR2

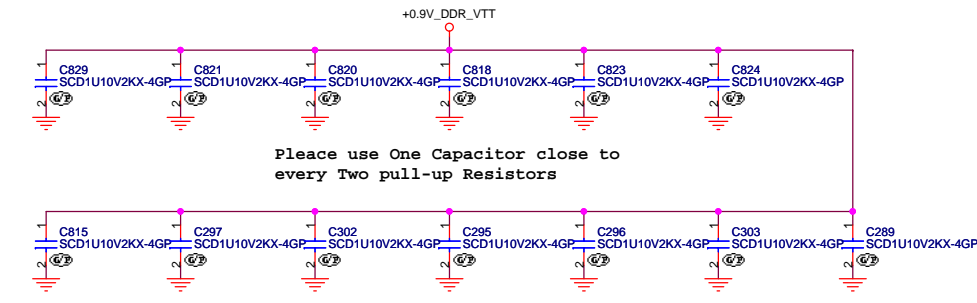


DIM2
DDR2-200P-8-GP-U1
62.10017.861

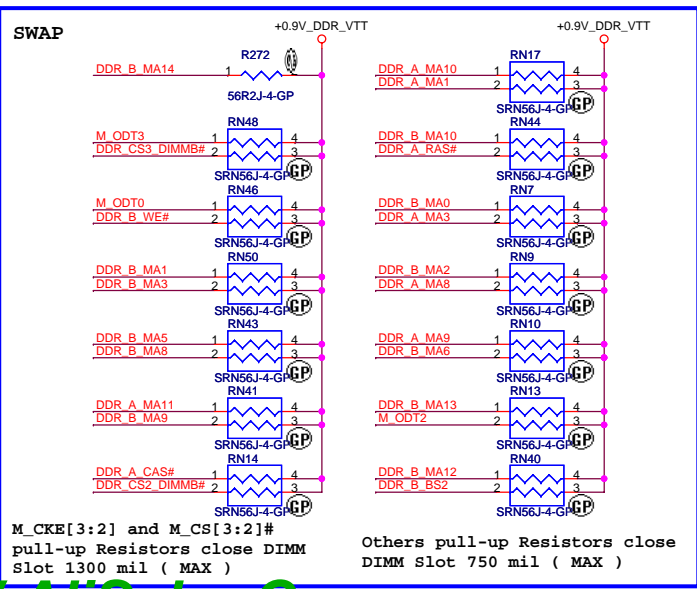
V_DDR_MCH_REF



Place close to the DIMM Slot



Place use One Capacitor close to every Two pull-up Resistors



M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)

Others pull-up Resistors close
DIMM slot 750 mil (MAX)

DDR_A_MA3 <<> DDR_A_MA3 9,13
DDR_A_MA1 <<> DDR_A_MA1 9,13
DDR_A_MA8 <<> DDR_A_MA8 9,13
DDR_A_MA9 <<> DDR_A_MA9 9,13
DDR_A_MA11 <<> DDR_A_MA11 9,13
DDR_A_MA10 <<> DDR_A_MA10 9,13
DDR_A_CAS# <<> DDR_A_CAS# 9,13
DDR_A_RAS# <<> DDR_A_RAS# 9,13
M_ODT0 <<> M_ODT0 8,13

DDR_CS2 DIMMB# <<> DDR_CS2 DIMMB# 8
DDR_CS3 DIMMB# <<> DDR_CKE2 DIMMB 8,13
DDR_CKE2 DIMMB <<> DDR_CKE3 DIMMB 8,13
DDR_CKE3 DIMMB <<> DDR_B_RAS# 9,13
DDR_B_RAS# <<> DDR_B_CAS# 9,13
DDR_B_WE# <<> DDR_B_WE# 9
M_ODT2 <<> M_ODT2 8
M_ODT3 <<> M_ODT3 8

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Title **DDR2-SODIMM2**

Size A3	Document Number	Rev SA
Siberia / Converse		

Date: Friday, September 01, 2006 Sheet 14 of 53



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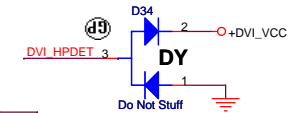
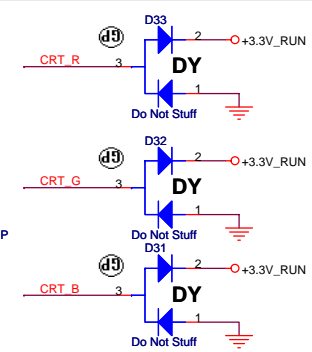


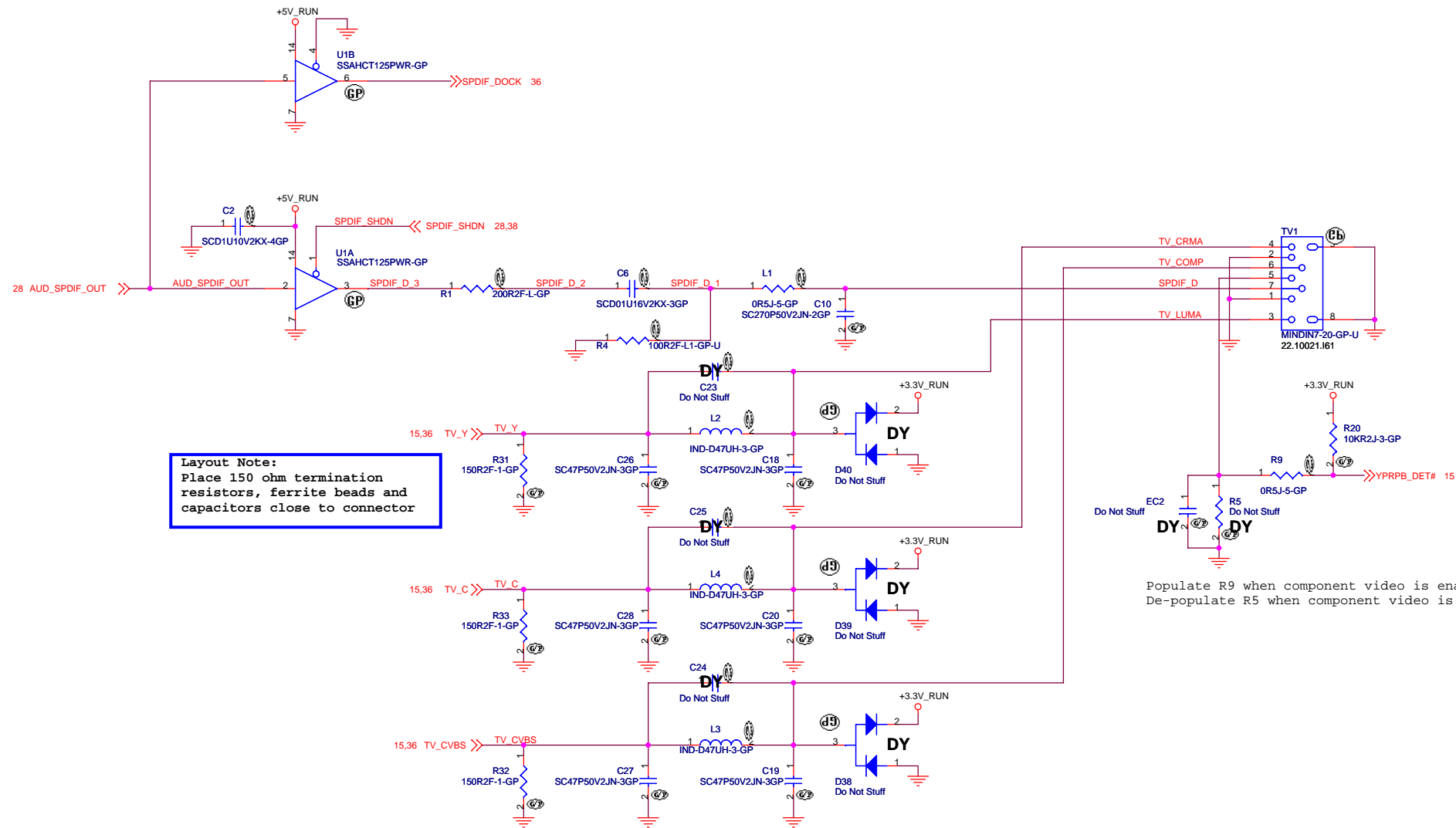
Graphic CONN.

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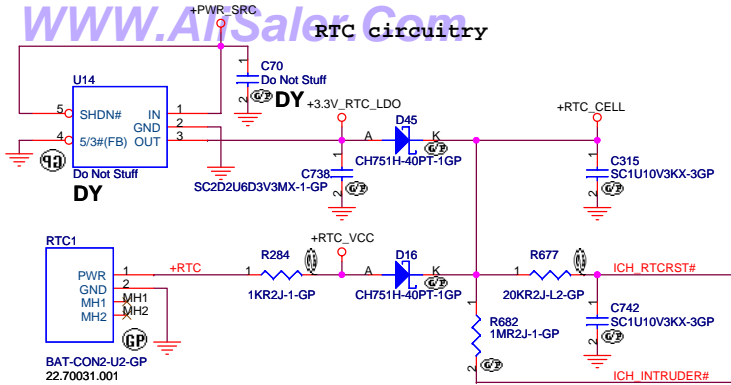




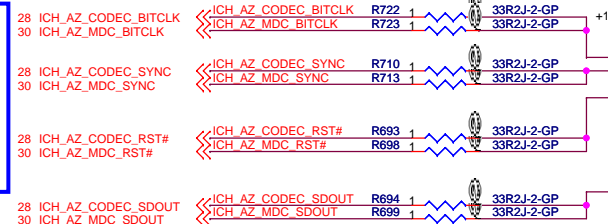
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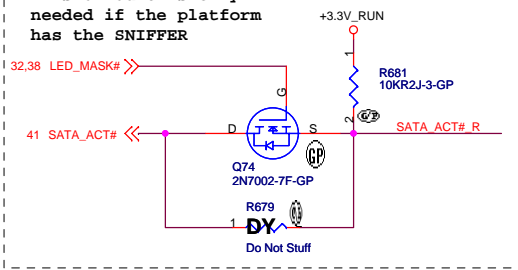
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TV OUT		
Size A3	Document Number	Rev SA
Date: Friday, September 01, 2006	Siberia / Converse	Sheet 17 of 53



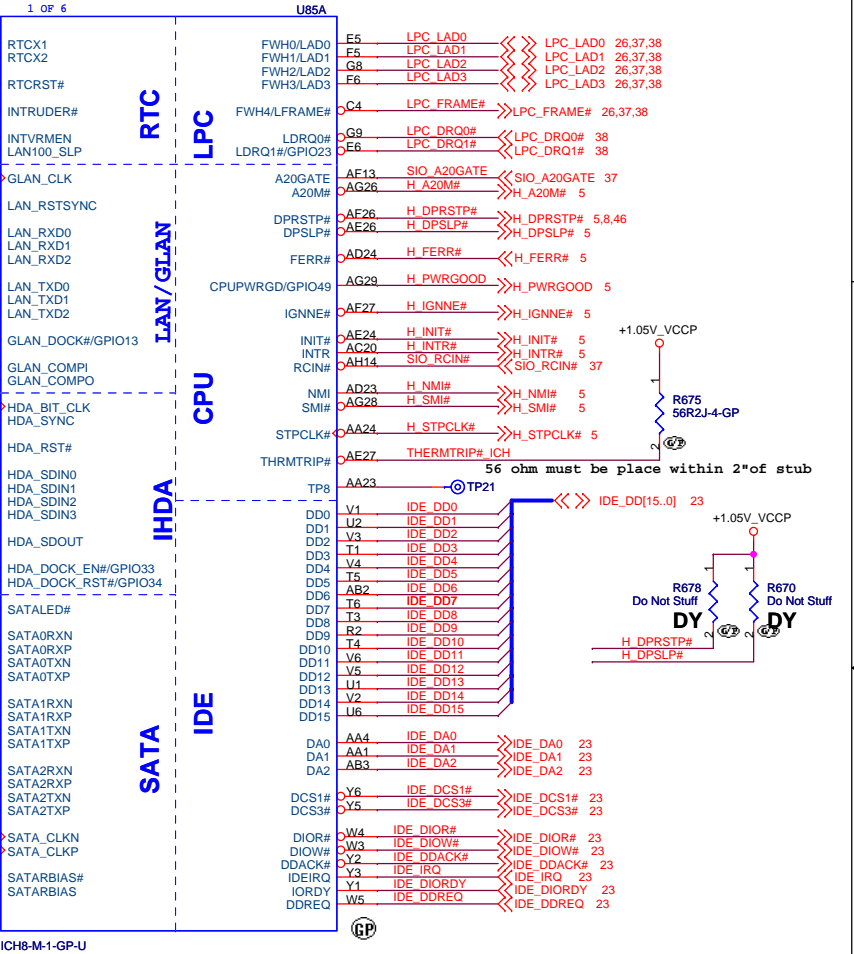
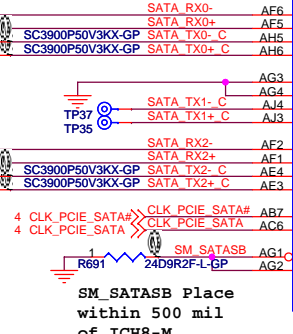
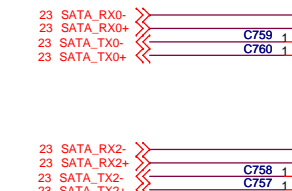
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R698, R699, R713 & R723 should equal distance to the split trace point as R693, R694, R710 & R722 respectively. Basically, keep the same distance from T for all series termination resistors.



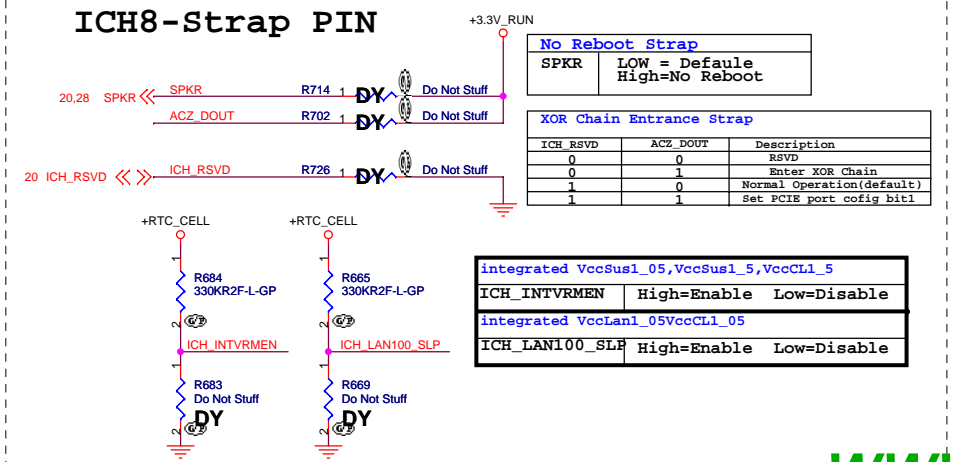
This circuit is only needed if the platform has the SNIFFER



Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.



ICH8-Strap PIN



No Reboot Strap	
SPKR	LOW = Default High = No Reboot

XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (default)
1	1	Set PCIE port config bit1

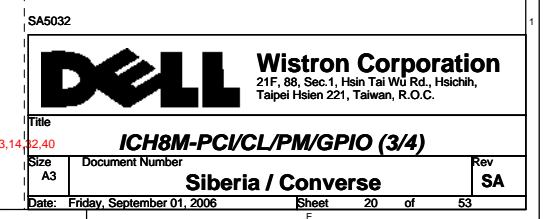
integrated VccSus1_05, VccSus1_5, VccCL1_5		
ICH_INTVRMEN	High=Enable Low=Disable	
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable Low=Disable	

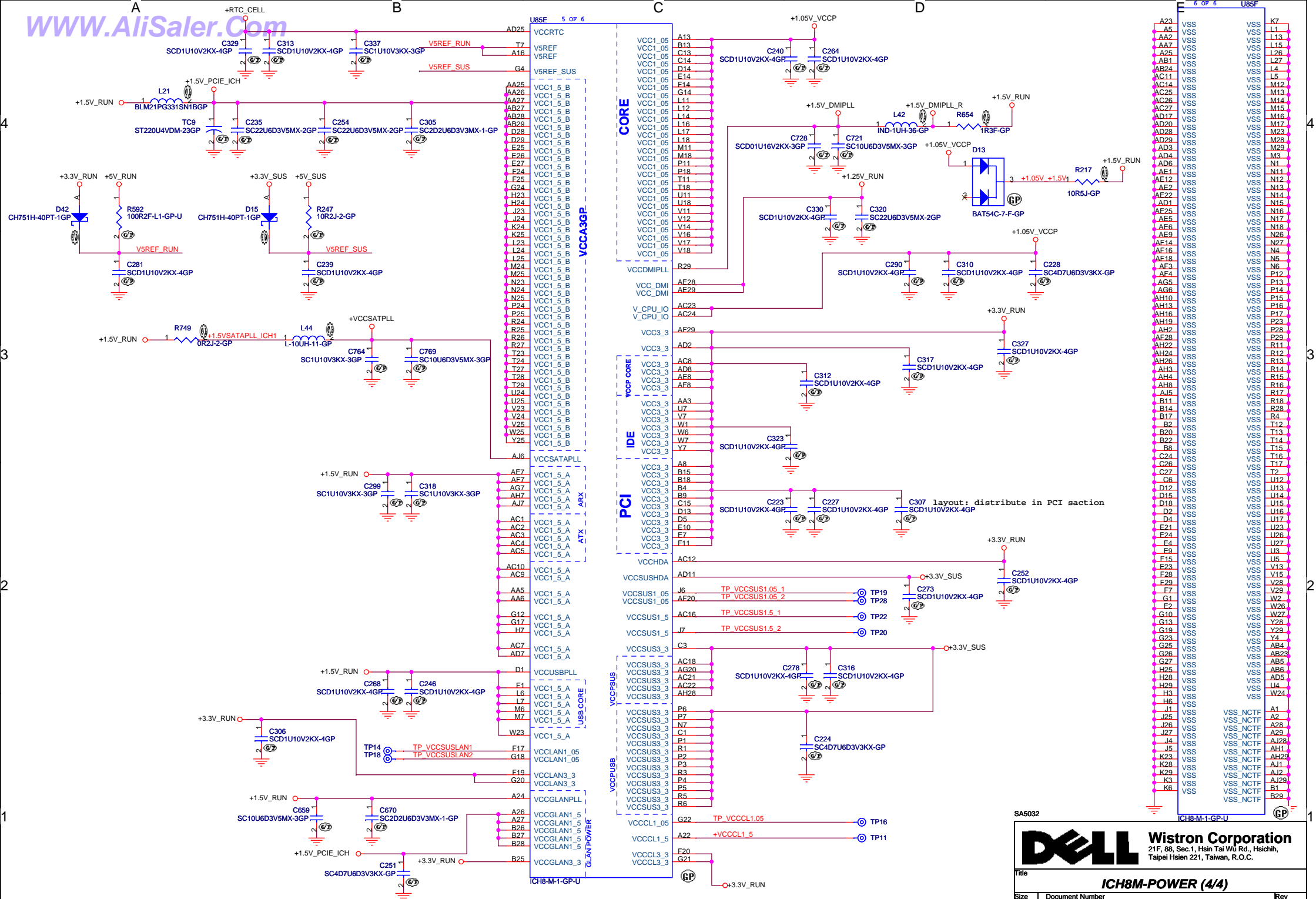
SA5032



Title		
ICH8M-RTC/IDE/LPC/DHI (1/4)		
Size A3	Document Number	Rev SA
Siberia / Converse		
Date: Thursday, September 07, 2006	Sheet 18 of 53	

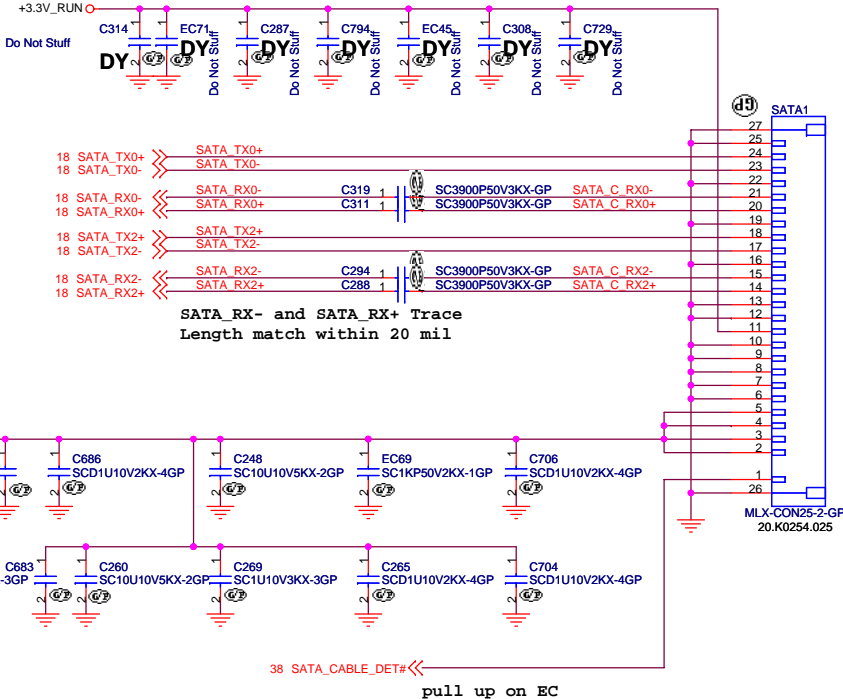
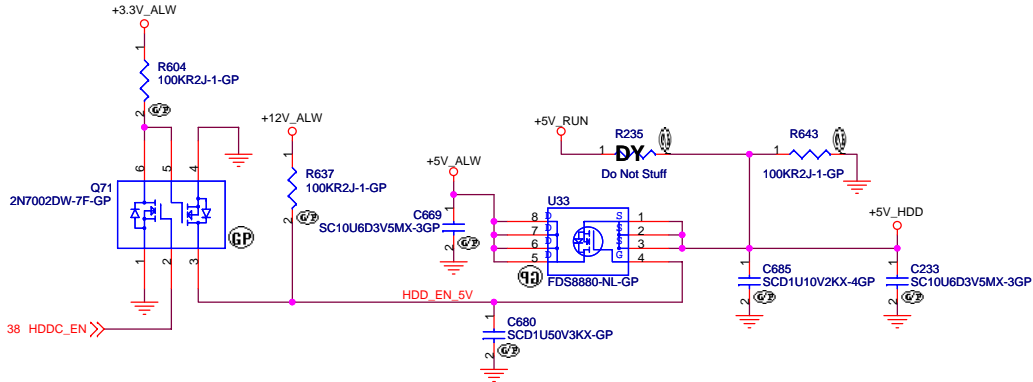
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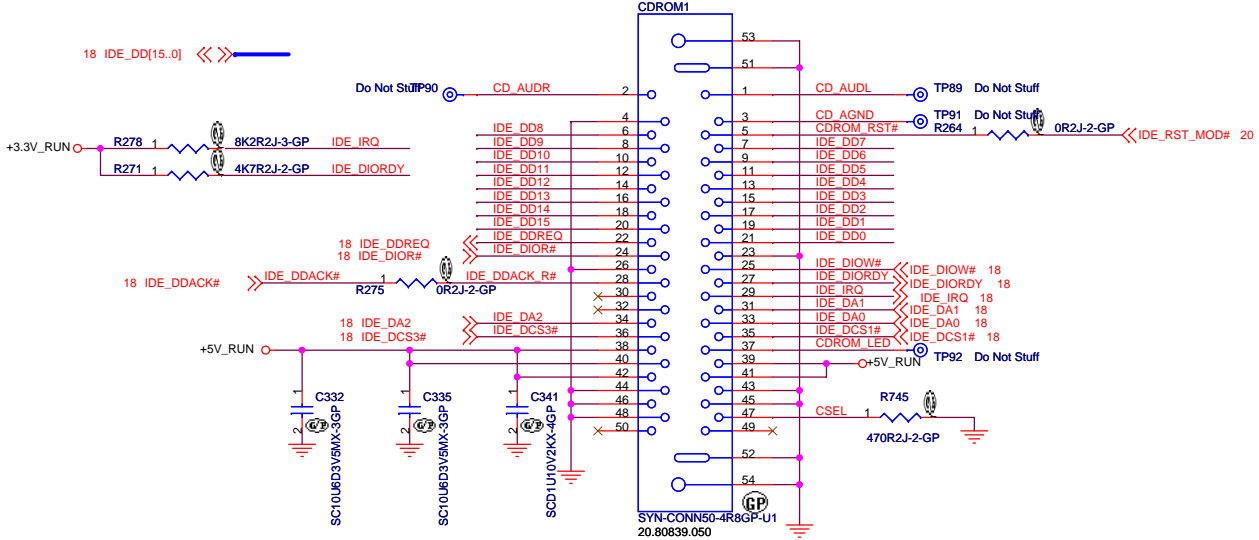




SATA HDD Connector



ODD Connector

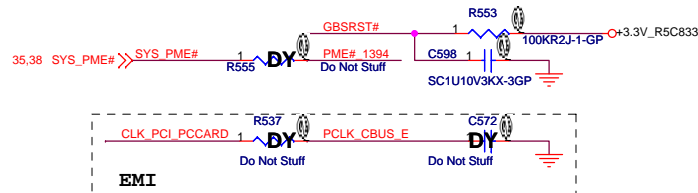


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Taipei Hsien 221, Taiwan, R.O.C.

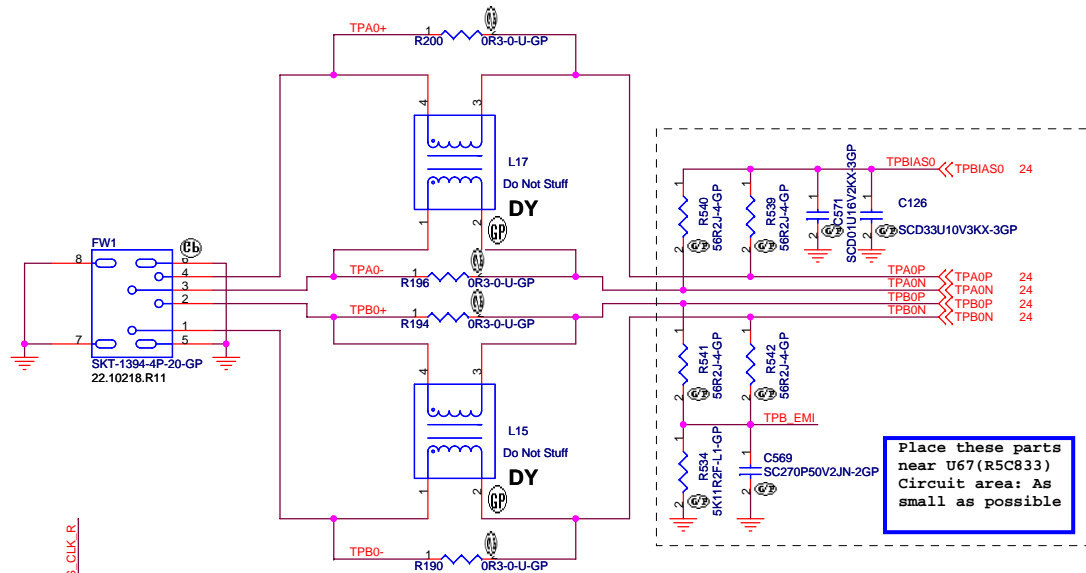
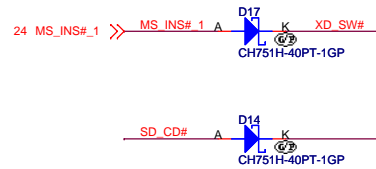
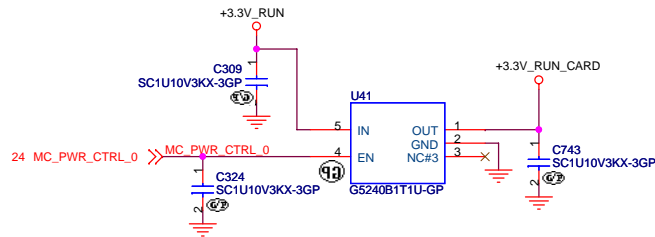
Title **HDD&ODD**

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Date: Friday, September 01, 2006	Sheet 23 of 53	

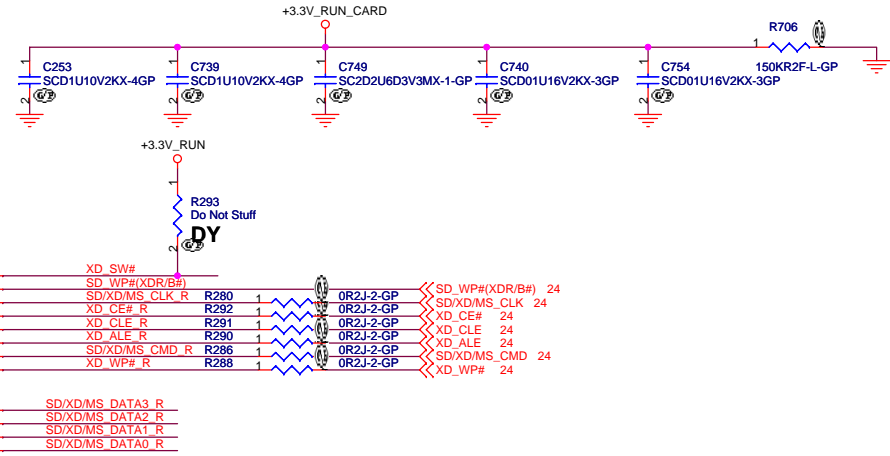
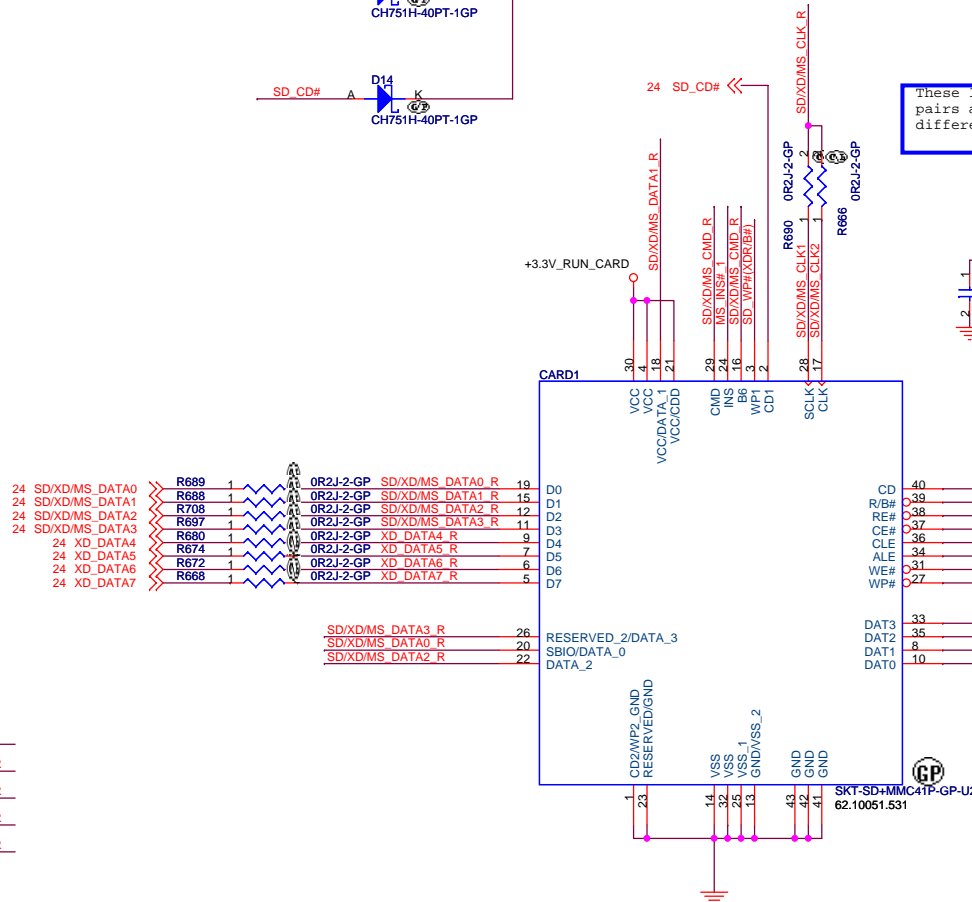


SA5032			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1394 - R5C832			
Size A3	Document Number	Rev SA	
Siberia / Converse			
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SSID = 1394



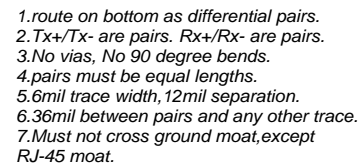
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance(Z_0) of 110 ohms.



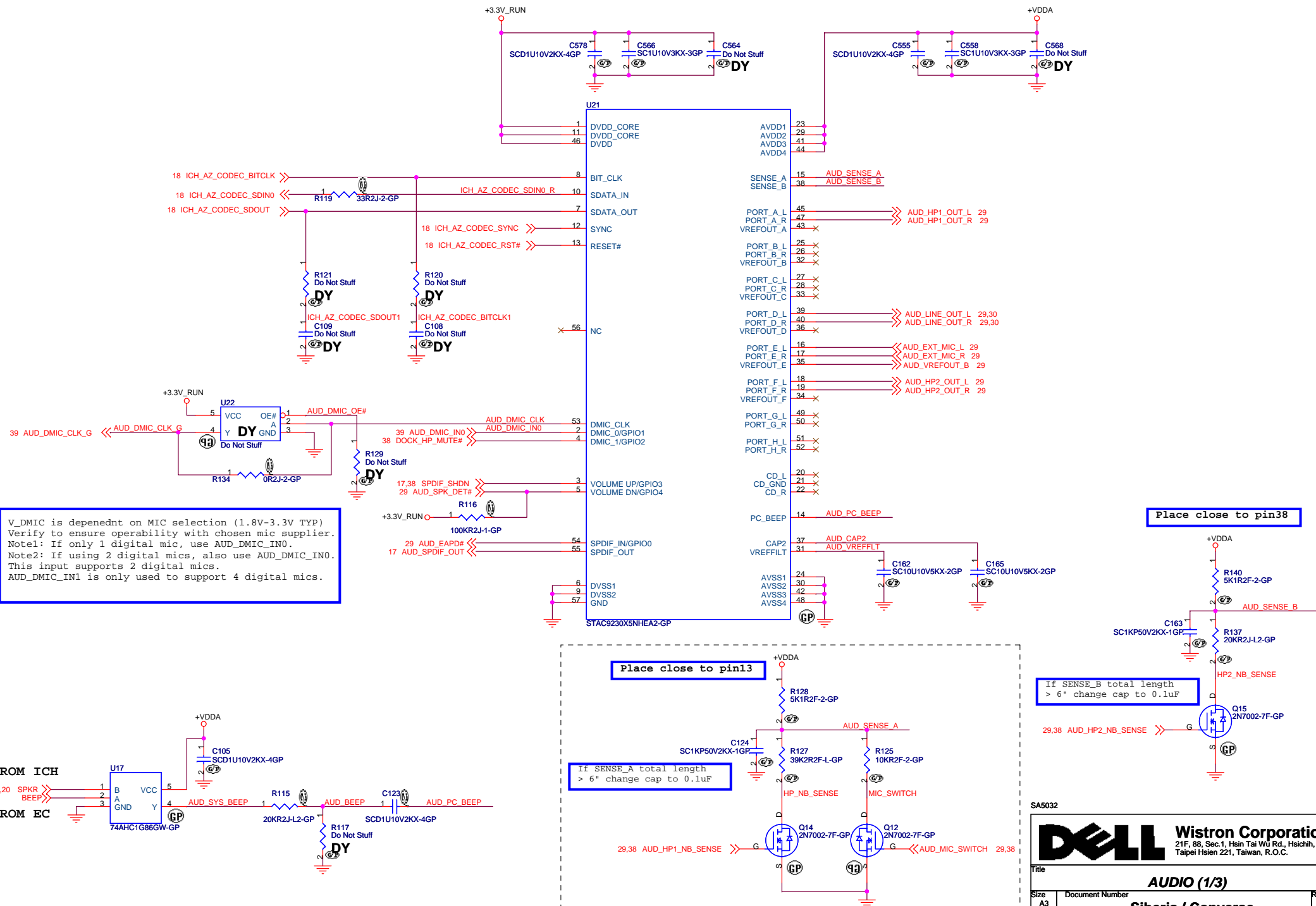
SA5032

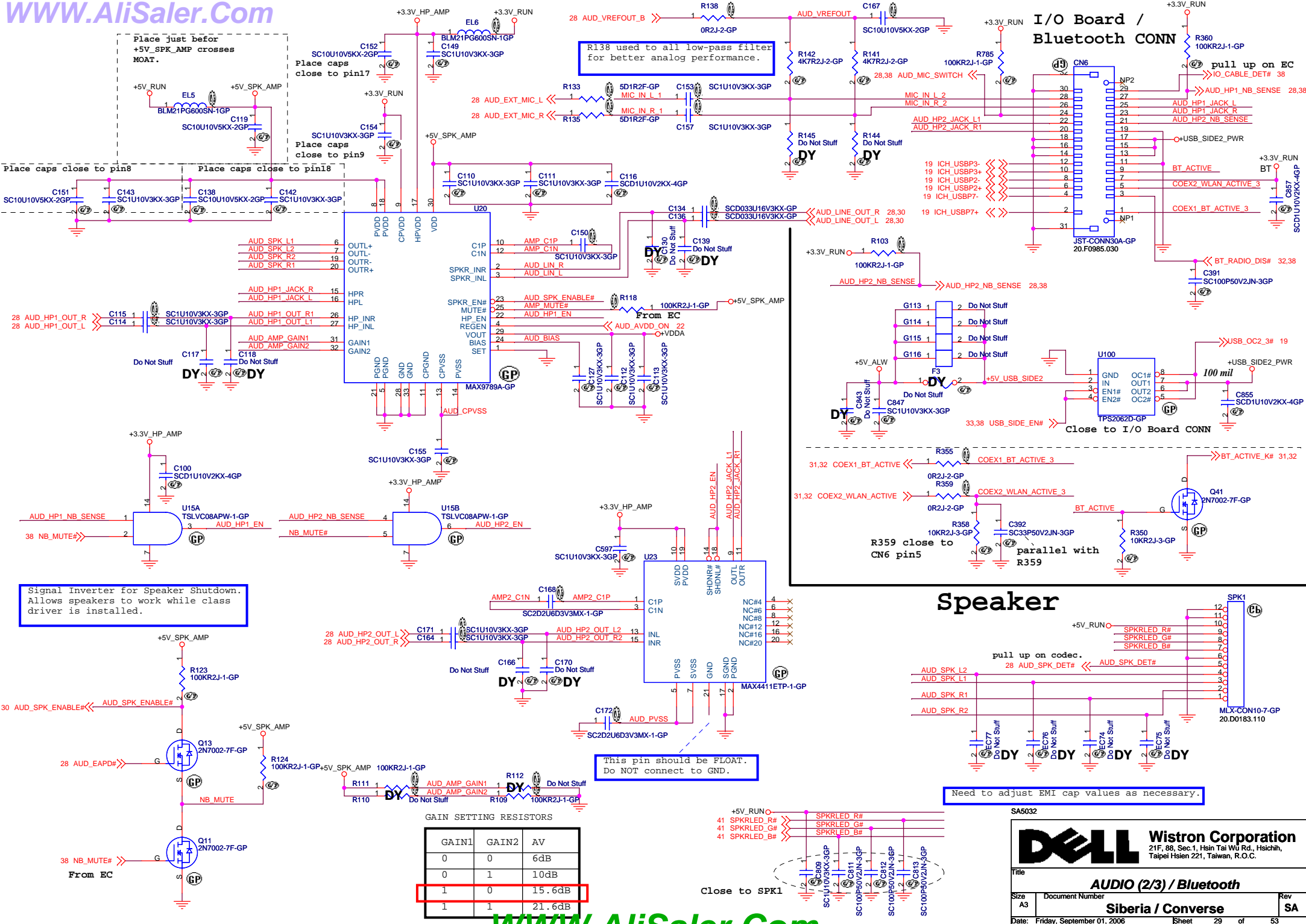
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

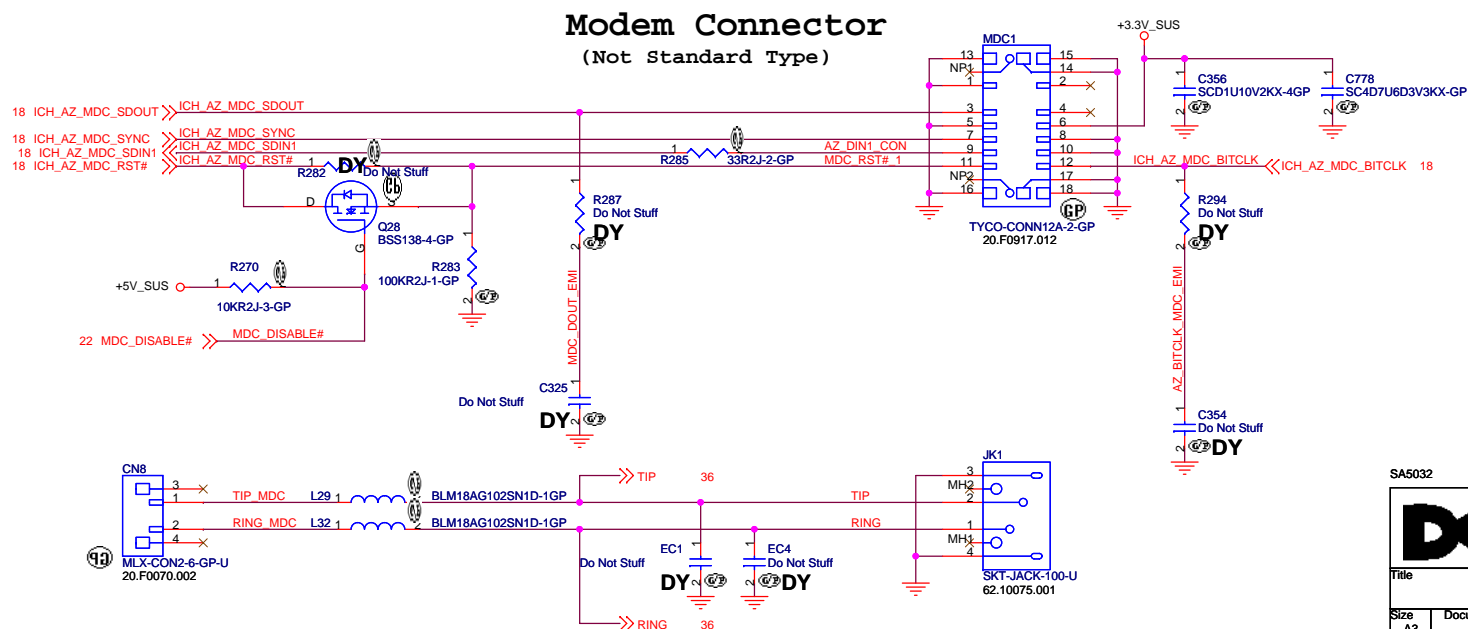
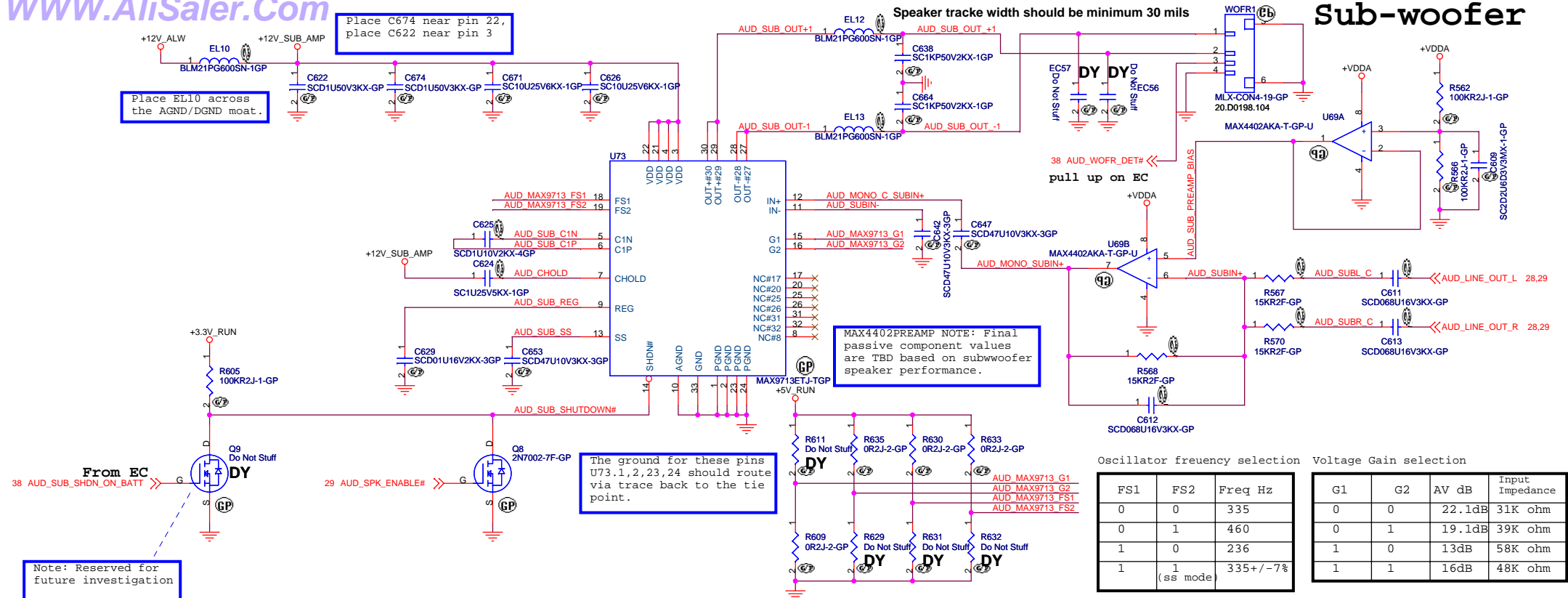
Title: 1394 - 8 IN 1 Connector
Size: A3 Document Number: Siberia / Converse Rev: SA
Date: Friday, September 01, 2006 Sheet: 25 of 53

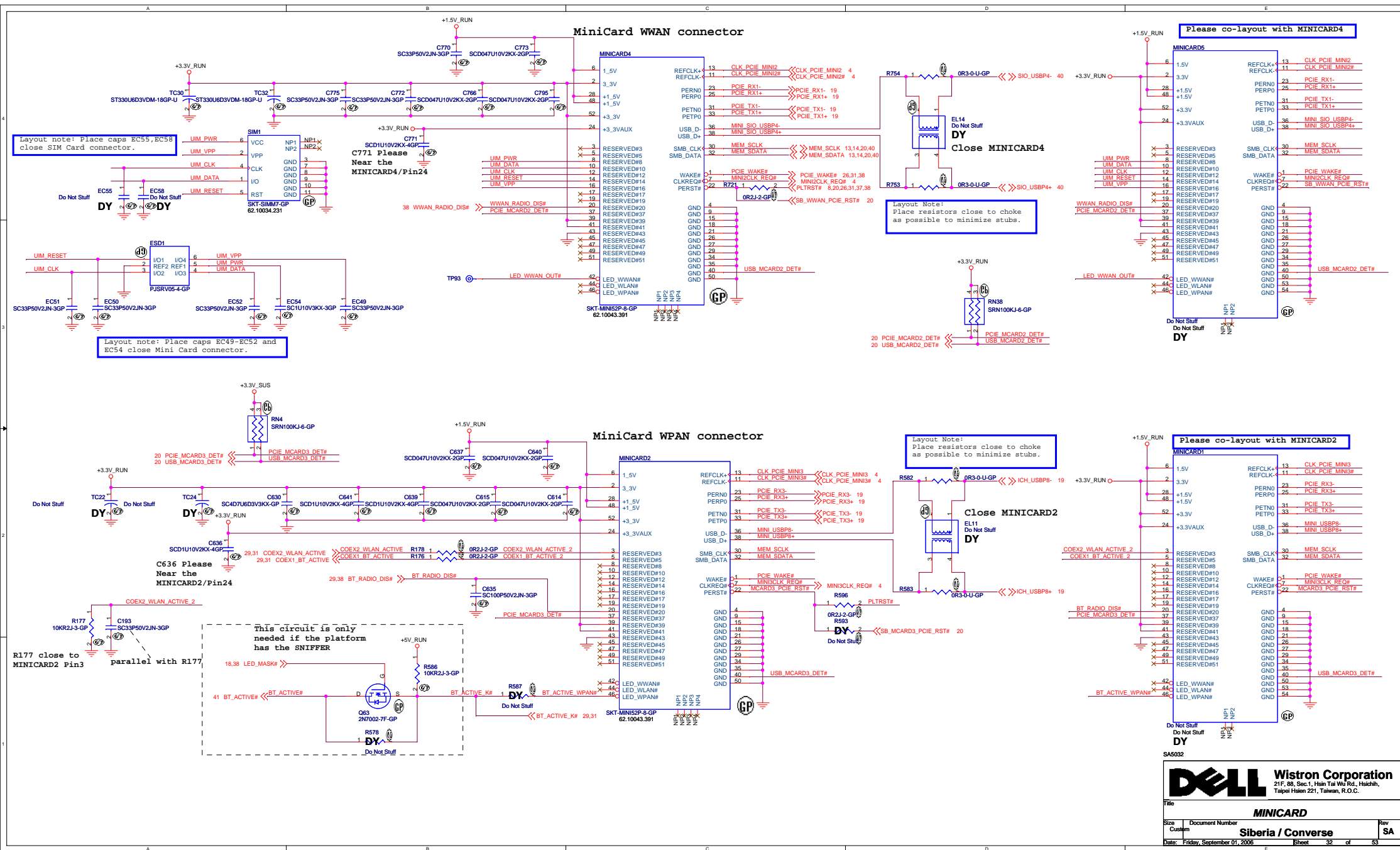


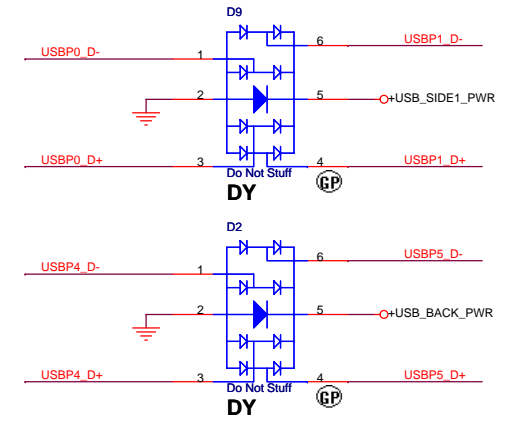
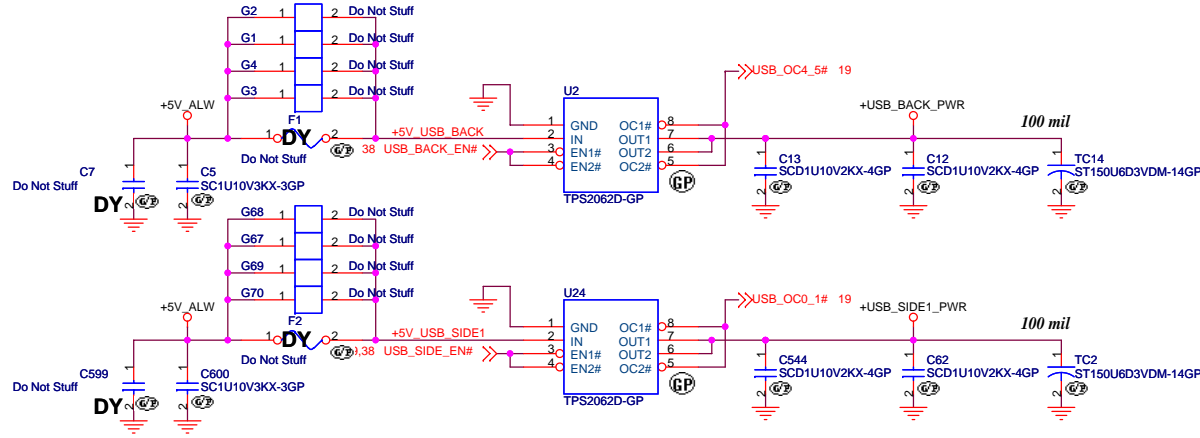
Rj11 layout guide line update > 100mil





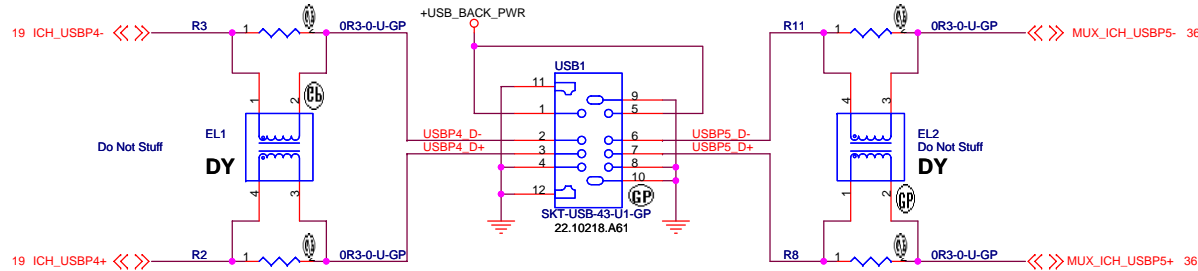




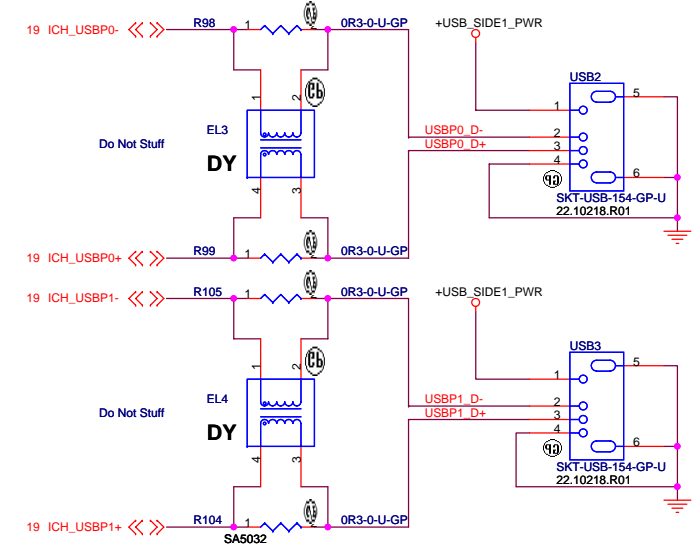


Place ESD diodes as close to the connector as possible.

USB PORT(BACK Port)

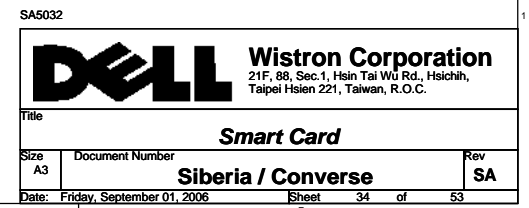


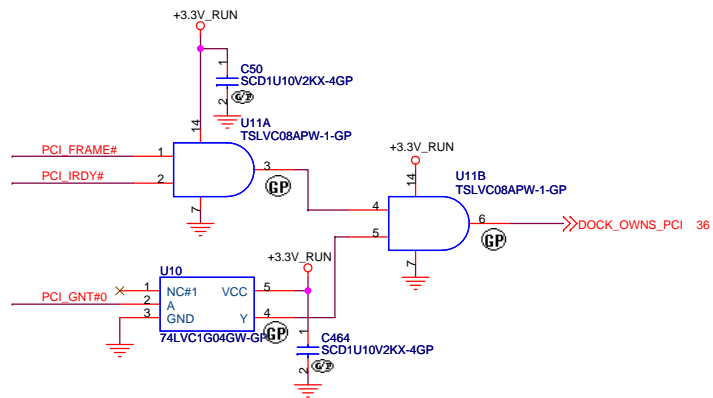
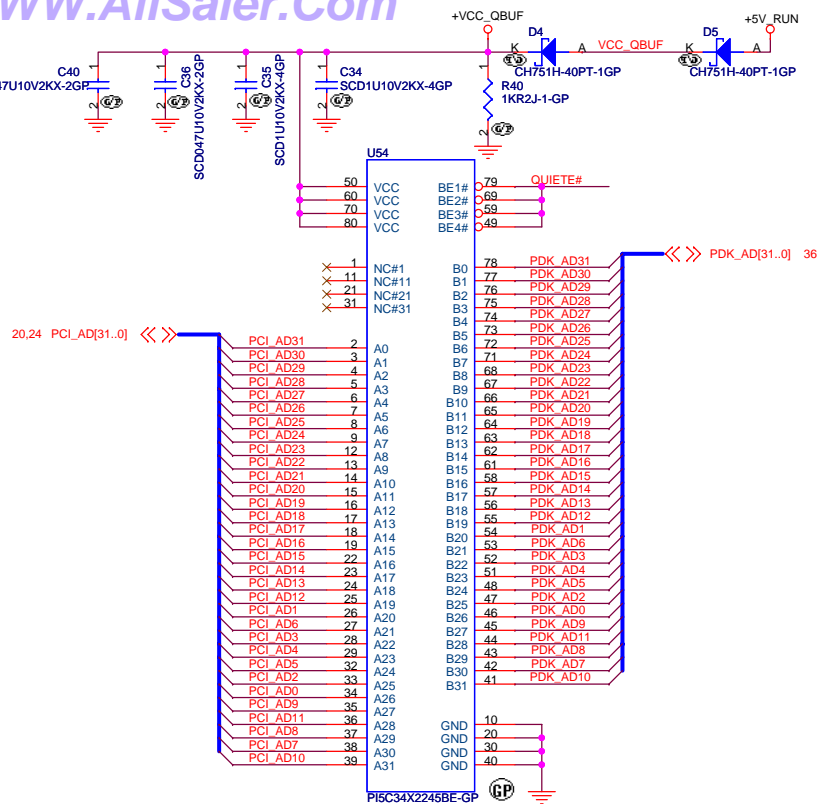
USB PORT(SIDE Port)



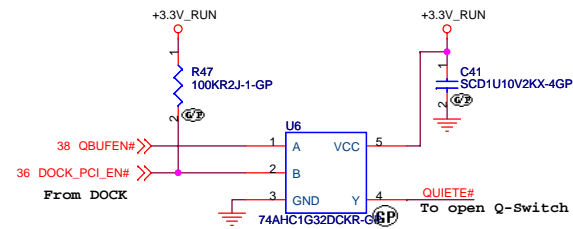
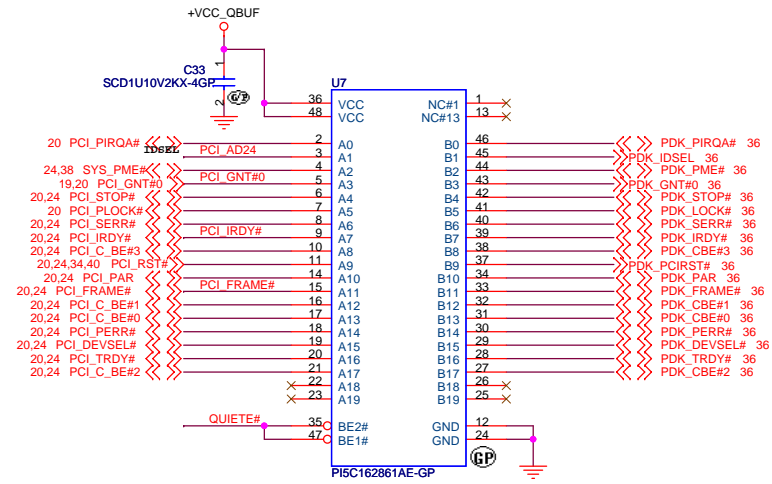
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Title			USB PORT	
Size	Document Number	Siberia / Converse		Rev
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D-DOCK Q ' SW



Dock on sequence

- ```
* BIOS request through SMB to connect to PCI bus in the dock
* D-dock state machine generates REQ 0
* ICH8 generates GNT0
* Notebook waits for next Idle bus cycle (IORDY# and FRAME#)
* DOCK_QWNS_PCI is generated
* on rising edge of PCI clock REQ0 is deasserted and
DOCK_PCI_EN# is asserted
* now Q-switch is enabled and PCI goes through to the dock
* D-dock reports connection through SMB
* re-enumeration is done by BIOS
```

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|     | Title |
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### ***D Dock Buffer***

| Size |
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| Document Number |
|-----------------|

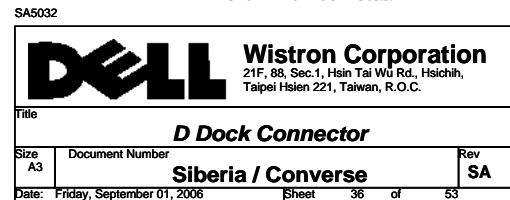
### Siberia / Converse

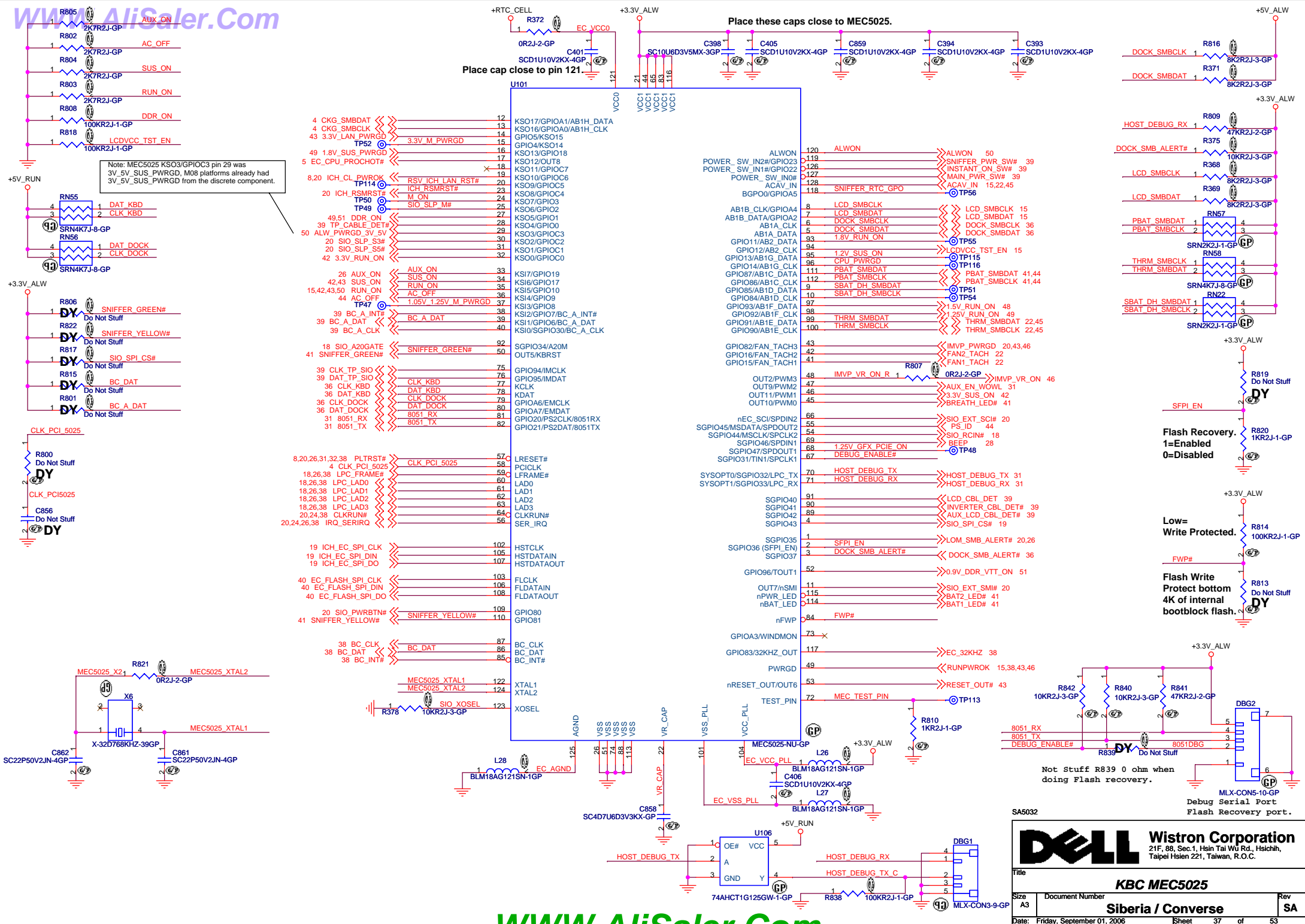
ev

Date: Friday, September 01, 2006

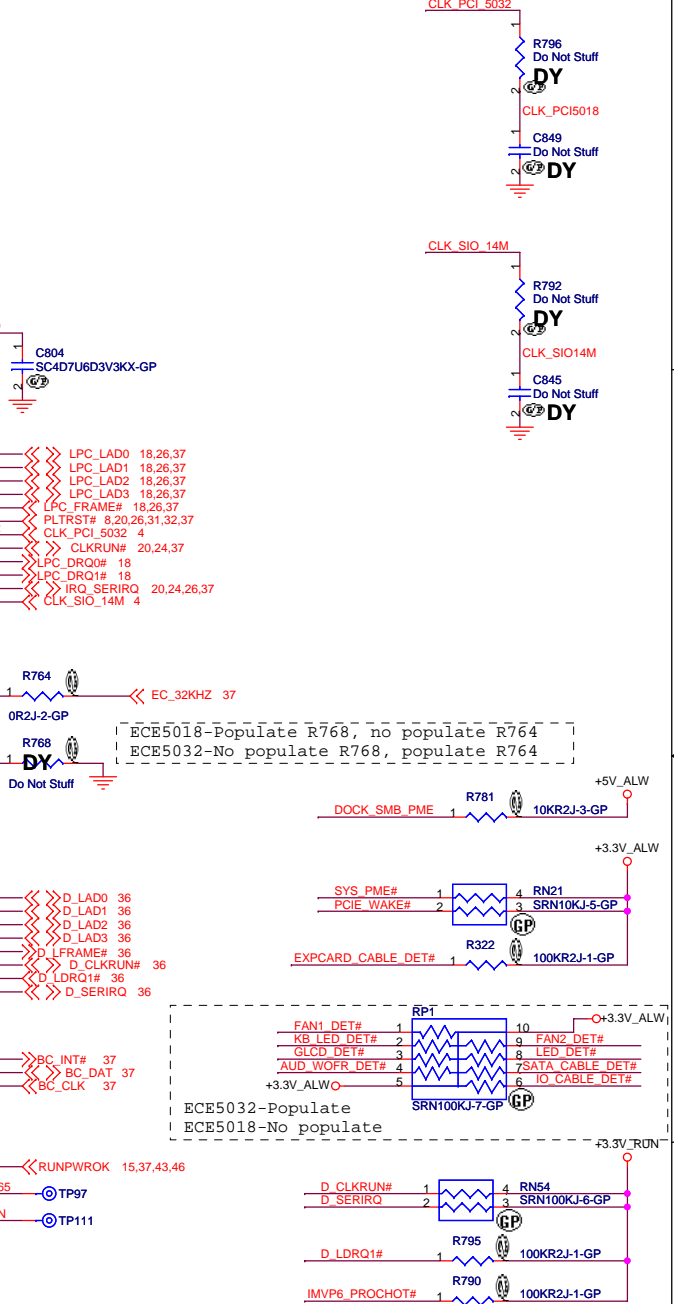
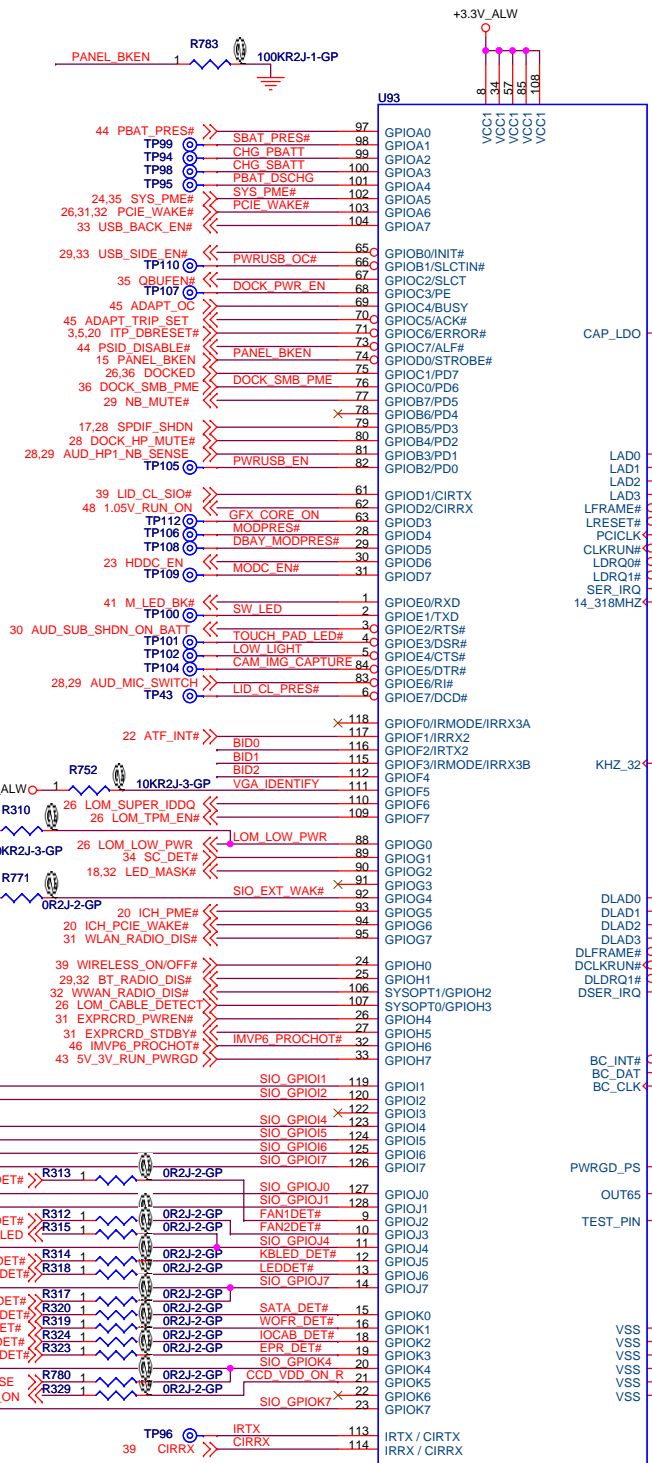
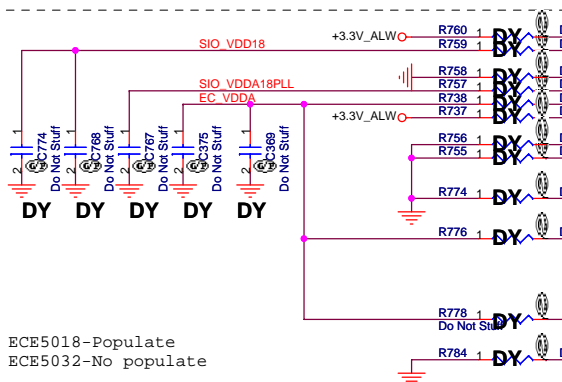
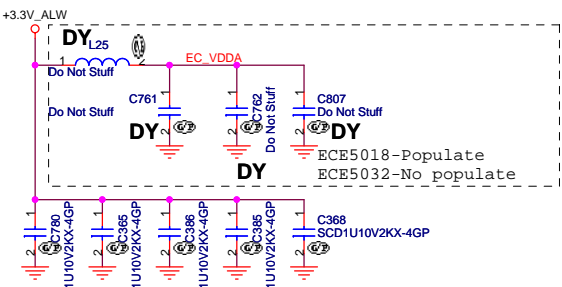
Sheet 35 of 53

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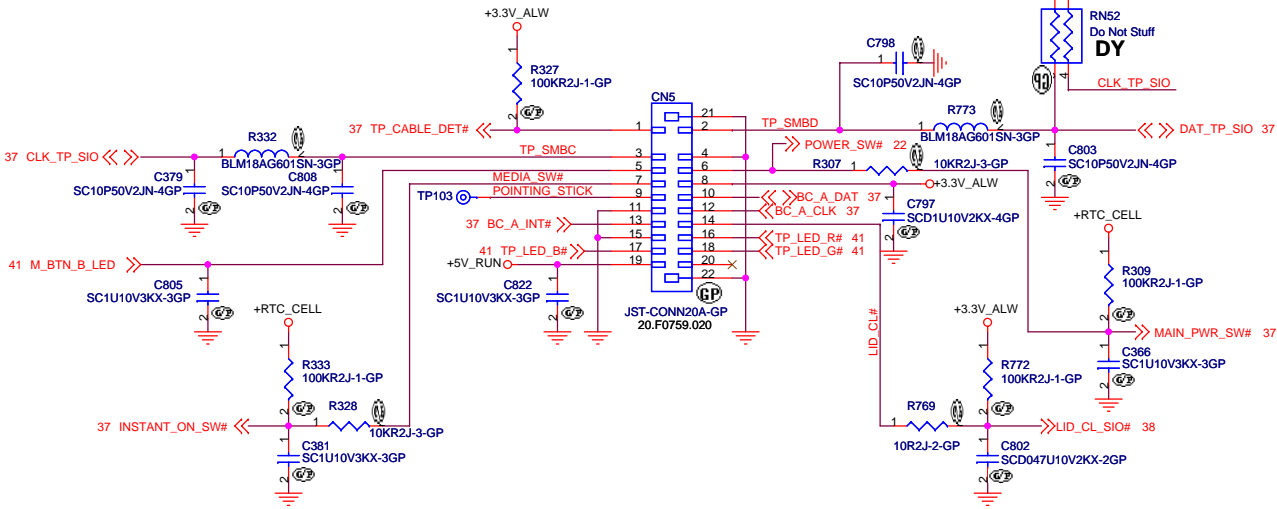
| BID2 | BID1 | BID0 | Board Rev. |
|------|------|------|------------|
| 0    | 0    | 0    | ENG1 (M00) |
| 0    | 0    | 1    | ENG2 (X00) |
| 0    | 1    | 0    | ENG3 (X01) |
| 0    | 1    | 1    | ENG4 (X02) |
| 1    | 0    | 0    | QT (X03)   |
| 1    | 0    | 1    | RAMP (A00) |
| 1    | 1    | 0    |            |



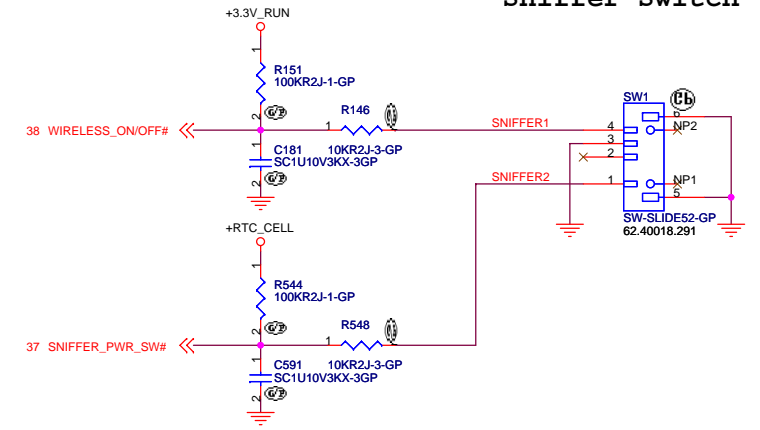
|                                                                                       |                            |                                                                                                             |          |
|---------------------------------------------------------------------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------|----------|
| SA5032                                                                                |                            |                                                                                                             |          |
|  |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title                                                                                 |                            |                                                                                                             |          |
| <b>SIO ECE5032</b>                                                                    |                            |                                                                                                             |          |
| Size<br>A3                                                                            | Document Number            | Rev                                                                                                         |          |
|                                                                                       | <b>Siberia / Converse</b>  | <b>SA</b>                                                                                                   |          |
| Date:                                                                                 | Friday, September 01, 2006 | Sheet                                                                                                       | 38 of 53 |



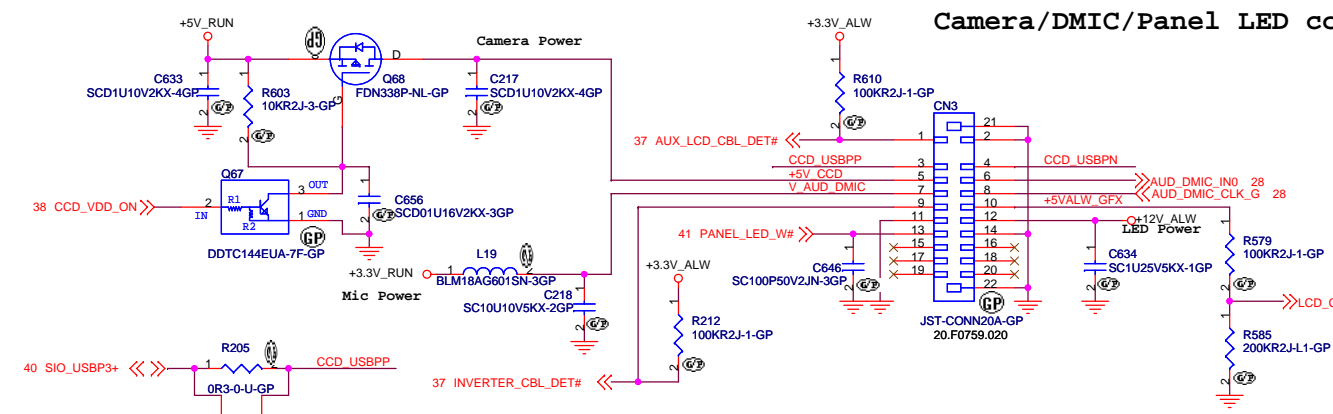
# Touch PAD conn.



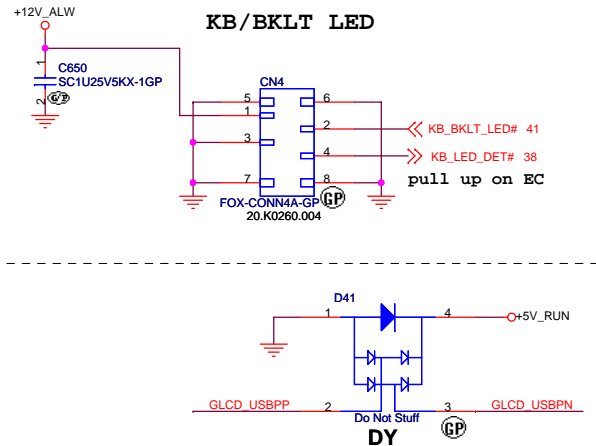
# Sniffer Switch



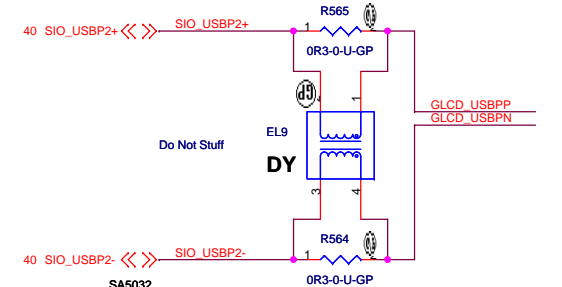
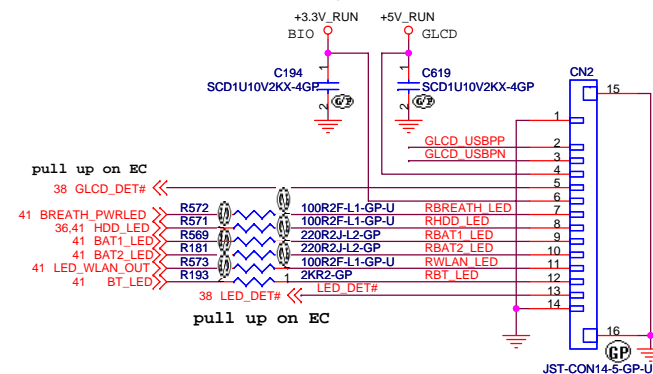
# Camera/DMIC/Panel LED conn.



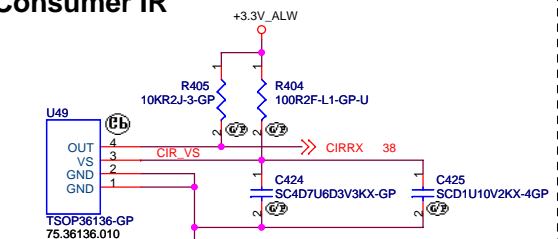
# KB/BKLT LED



# Indicator LED, Gaming LCD and Biometric reader conn.



# Consumer IR



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Title **Touch PAD/Gaming LCD/Biometric/CIR**

|                                  |                 |        |
|----------------------------------|-----------------|--------|
| Size A3                          | Document Number | Rev SA |
| Date: Friday, September 01, 2006 | Sheet 39 of 53  |        |

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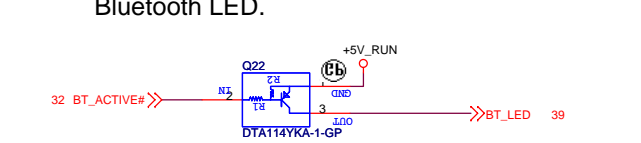
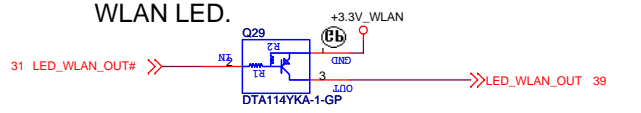
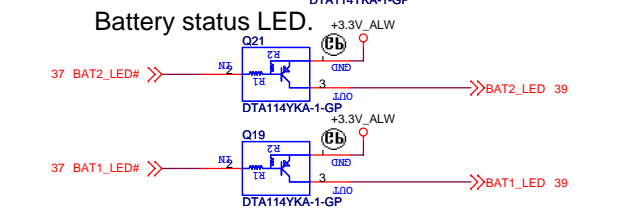
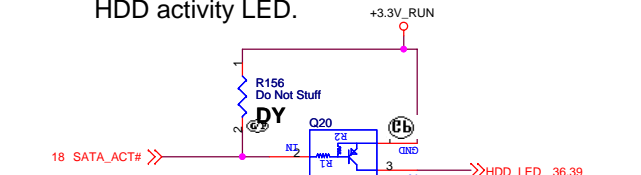
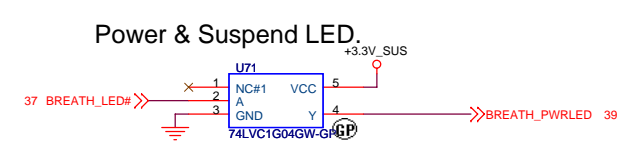
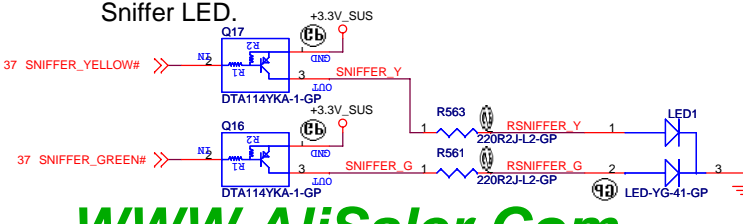
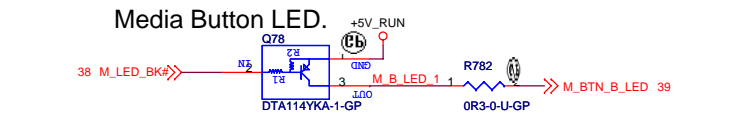
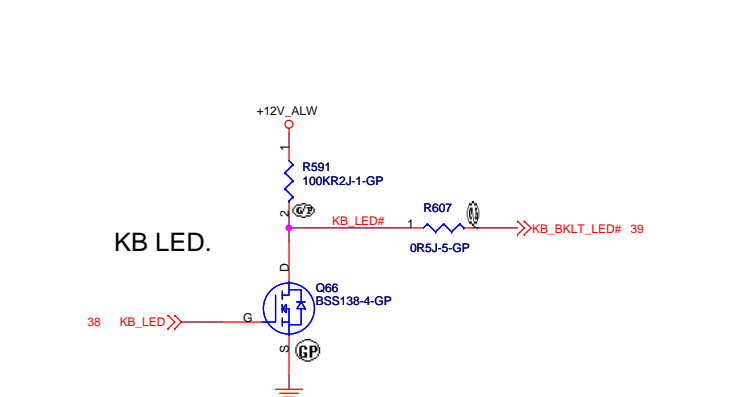
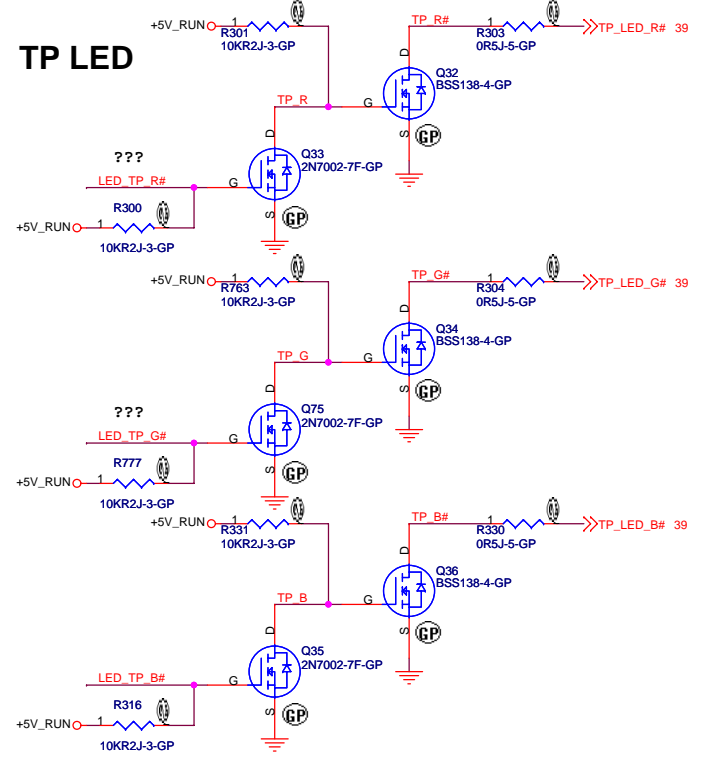
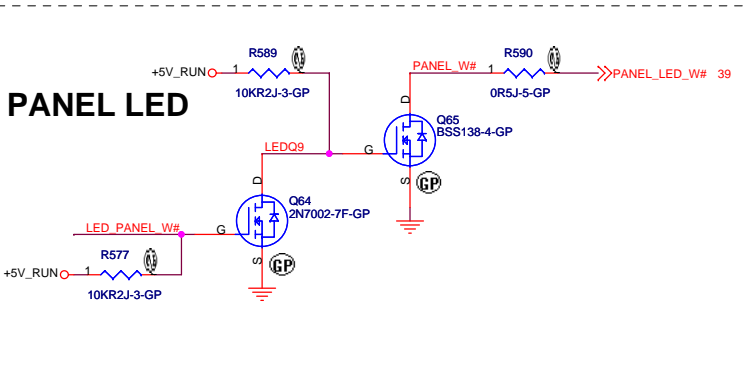
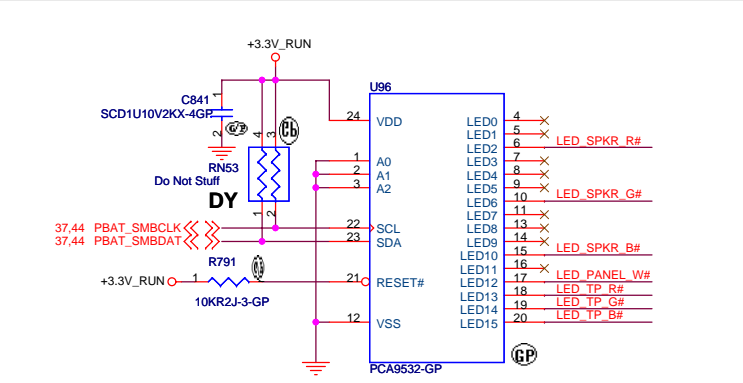
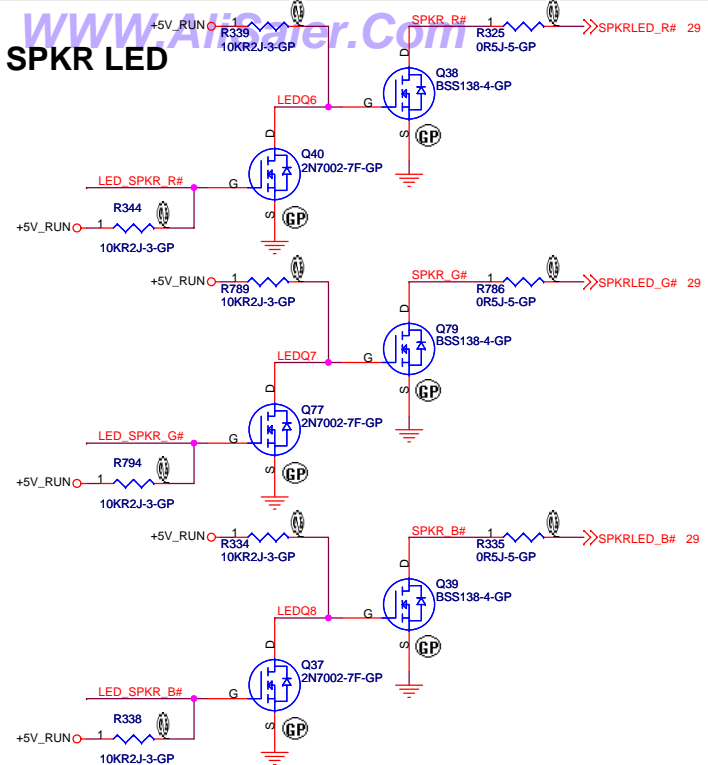
## SPI FLASH/USB HUB

## Siberia / Converse

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3





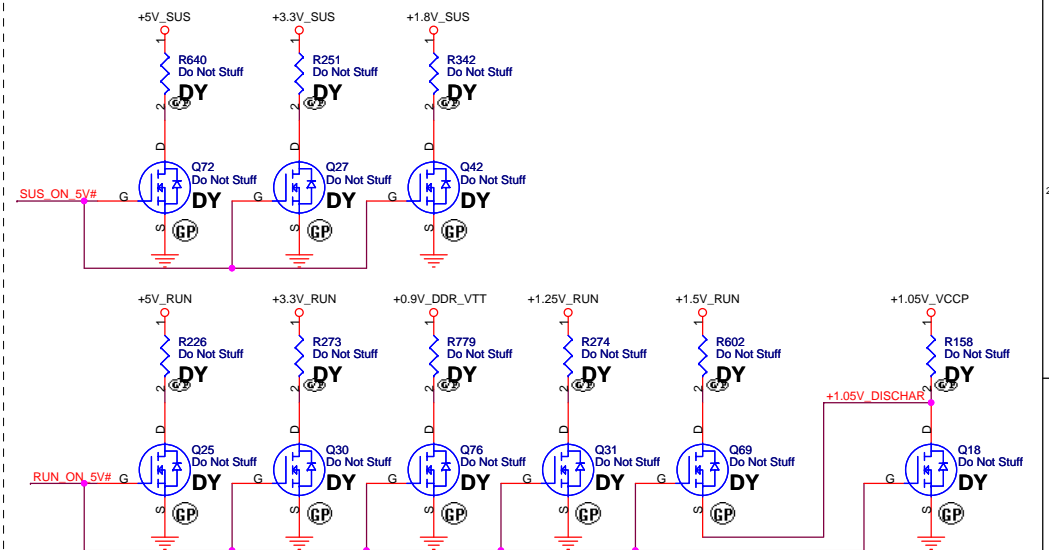
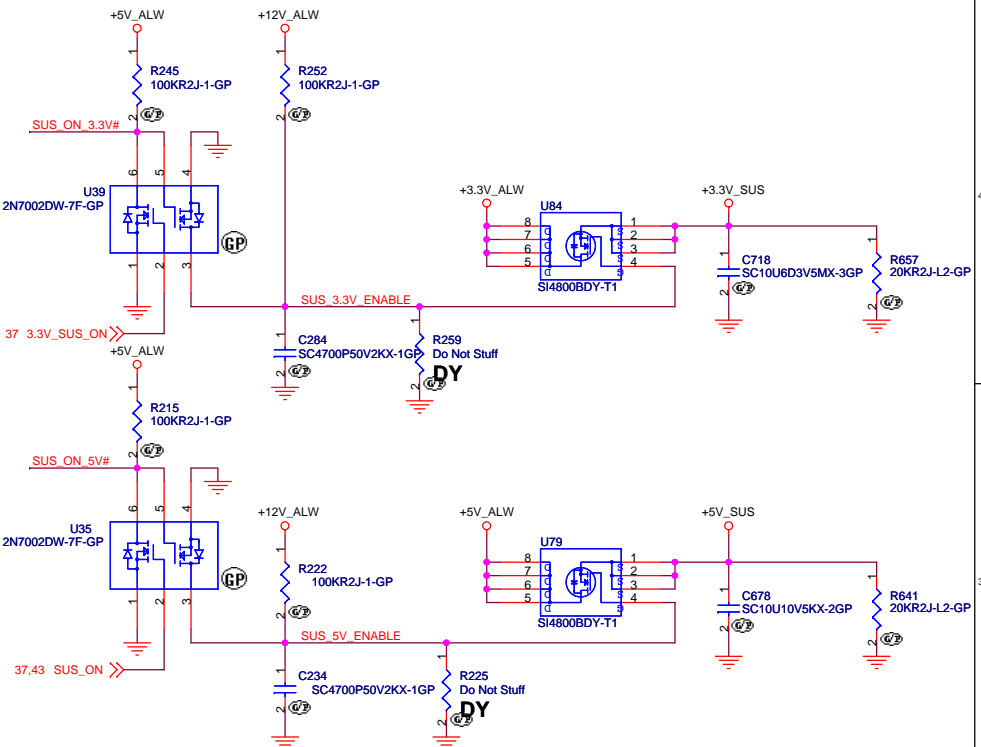
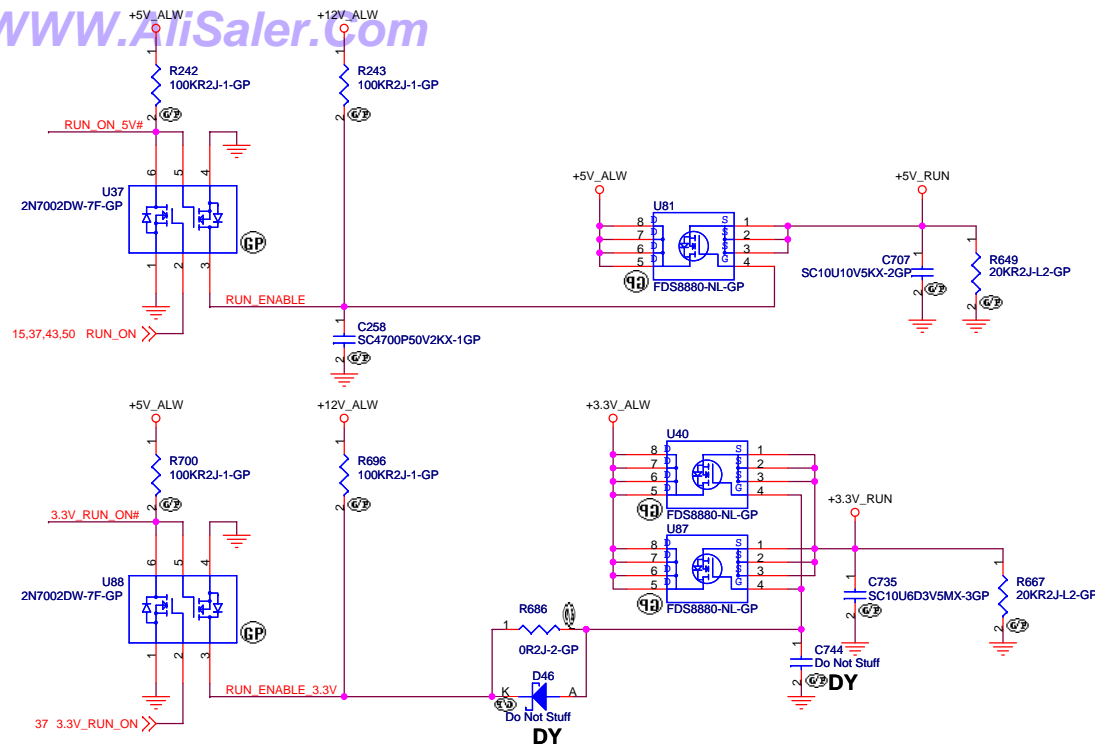
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Title: **LED**

Size: A3 Document Number: **Siberia / Converse** Rev: SA

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### Reserve discharge path

CRB 0.95:  
Insures that +1.05\_VCCP and +1.5\_RUN ramp down together by discharging +1.5V\_RUN into +1.05V\_VCCP

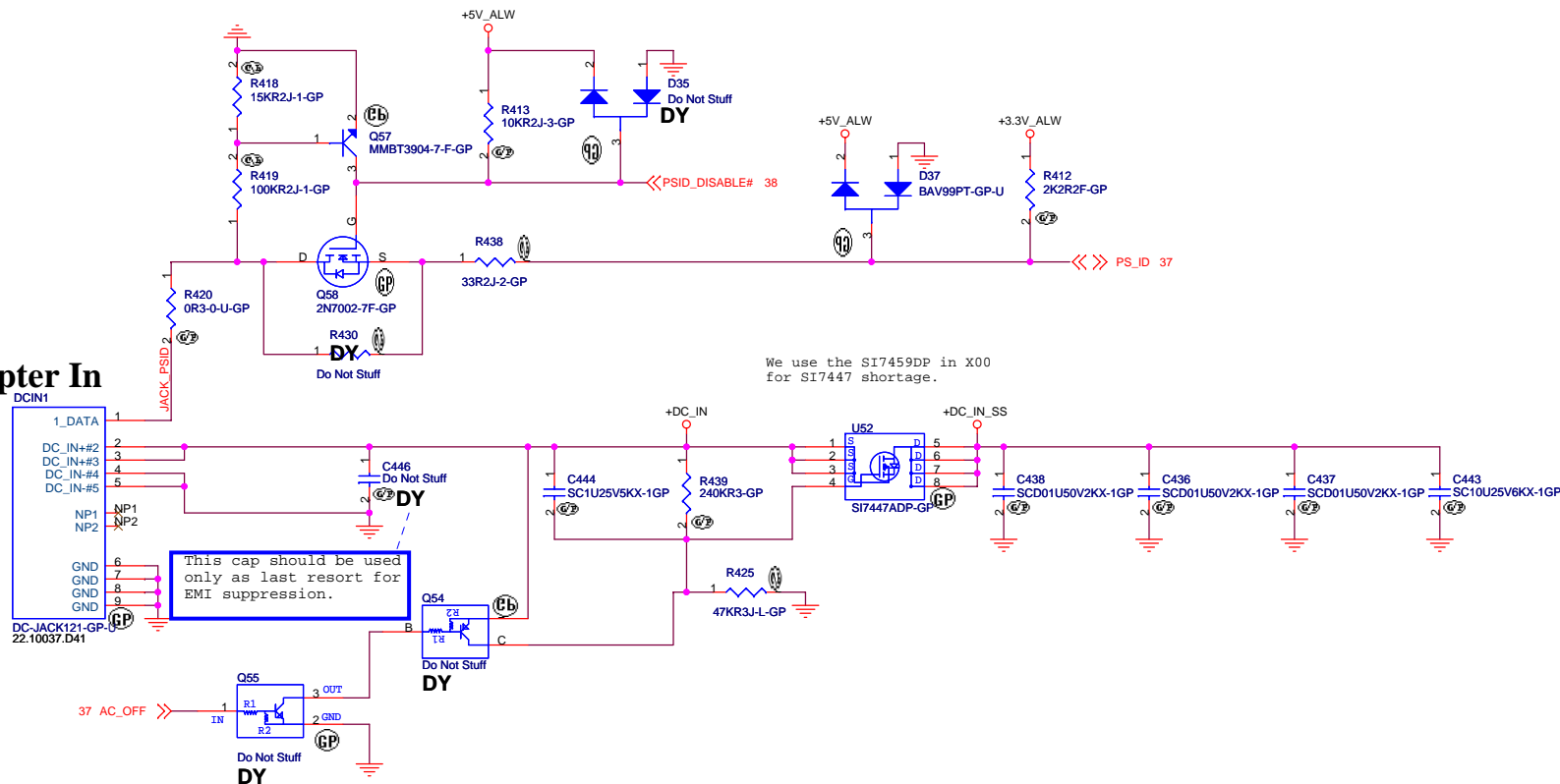
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|                                                                                                           |                 |        |
|-----------------------------------------------------------------------------------------------------------|-----------------|--------|
| <b>Wistron Corporation</b><br>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                 |        |
| Title                                                                                                     |                 |        |
| Power Plane Enable                                                                                        |                 |        |
| Size A3                                                                                                   | Document Number | Rev SA |
| Date: Friday, September 01, 2006                                                                          | Sheet 42 of 53  |        |

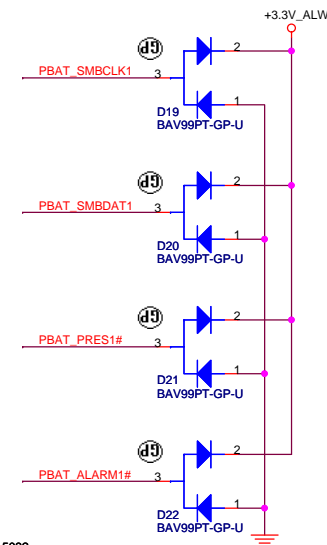
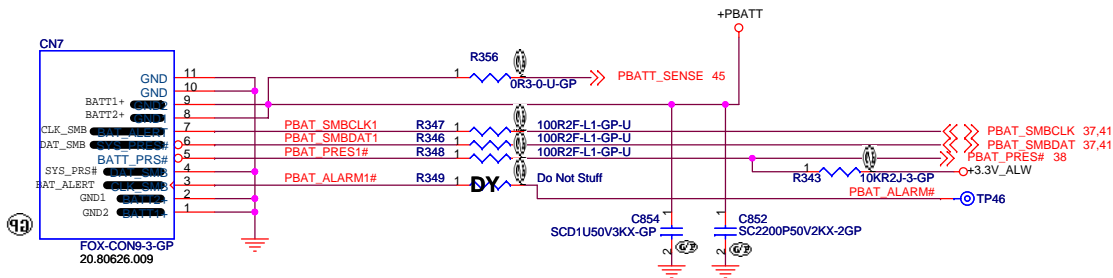




## Adapter In



## Batt Connector



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|       |                            |                    |                          |       |
|-------|----------------------------|--------------------|--------------------------|-------|
| Title |                            |                    | <b>DCIN / BATT CONN.</b> |       |
| Size  | Document Number            | Siberia / Converse |                          | Rev   |
| A3    |                            |                    |                          | SA    |
| Date: | Friday, September 01, 2006 | Sheet              | 44                       | of 53 |

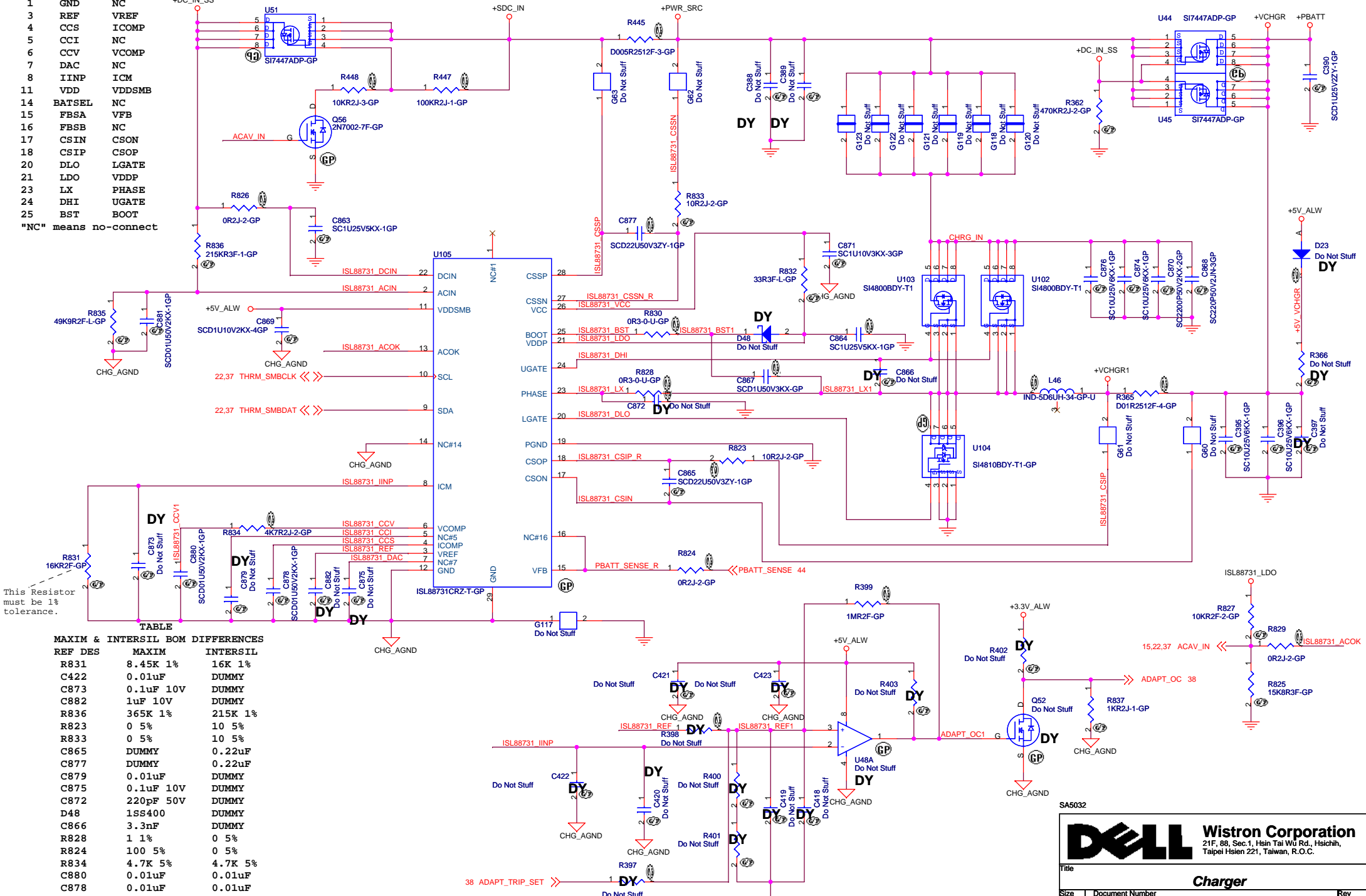
**\*PIN NAME DIFFERENCES\***

| PIN | MAXIM  | INTERSIL |
|-----|--------|----------|
| 1   | GND    | NC       |
| 3   | REF    | VREF     |
| 4   | CCS    | ICOMP    |
| 5   | CCI    | NC       |
| 6   | CCV    | VCOMP    |
| 7   | DAC    | NC       |
| 8   | IINP   | ICM      |
| 11  | VDD    | VDDSMB   |
| 14  | BATSEL | NC       |
| 15  | FBSA   | VFB      |
| 16  | FBSB   | NC       |
| 17  | CSIN   | CSOP     |
| 18  | CSIP   | CSOP     |
| 20  | DLO    | LGATE    |
| 21  | LDO    | VDDP     |
| 23  | LX     | PHASE    |
| 24  | DHI    | UGATE    |
| 25  | BST    | BOOT     |

"NC" means no-connect

We use the SI7459DP in X00 for SI7447 shortage.

We use the SI7459DP in X00 for SI7447 shortage.



TABLE

**MAXIM & INTERSIL BOM DIFFERENCES**

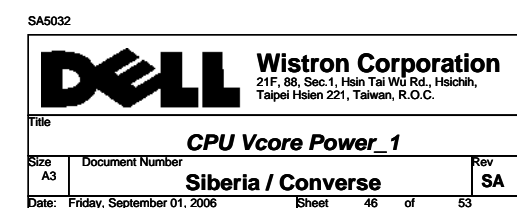
| REF  | DES | MAXIM     | INTERSIL |
|------|-----|-----------|----------|
| R831 |     | 8.45K 1%  | 16K 1%   |
| C422 |     | 0.01uF    | DUMMY    |
| C873 |     | 0.1uF 10V | DUMMY    |
| C882 |     | 1uF 10V   | DUMMY    |
| R836 |     | 365K 1%   | 215K 1%  |
| R823 |     | 0 5%      | 10 5%    |
| R833 |     | 0 5%      | 10 5%    |
| C865 |     | DUMMY     | 0.22uF   |
| C877 |     | DUMMY     | 0.22uF   |
| C879 |     | 0.01uF    | DUMMY    |
| C875 |     | 0.1uF 10V | DUMMY    |
| C872 |     | 220pF 50V | DUMMY    |
| D48  |     | 1SS400    | DUMMY    |
| C866 |     | 3.3nF     | DUMMY    |
| R828 |     | 1 1%      | 0 5%     |
| R824 |     | 100 5%    | 0 5%     |
| R834 |     | 4.7K 5%   | 4.7K 5%  |
| C880 |     | 0.01uF    | 0.01uF   |
| C878 |     | 0.01uF    | 0.01uF   |

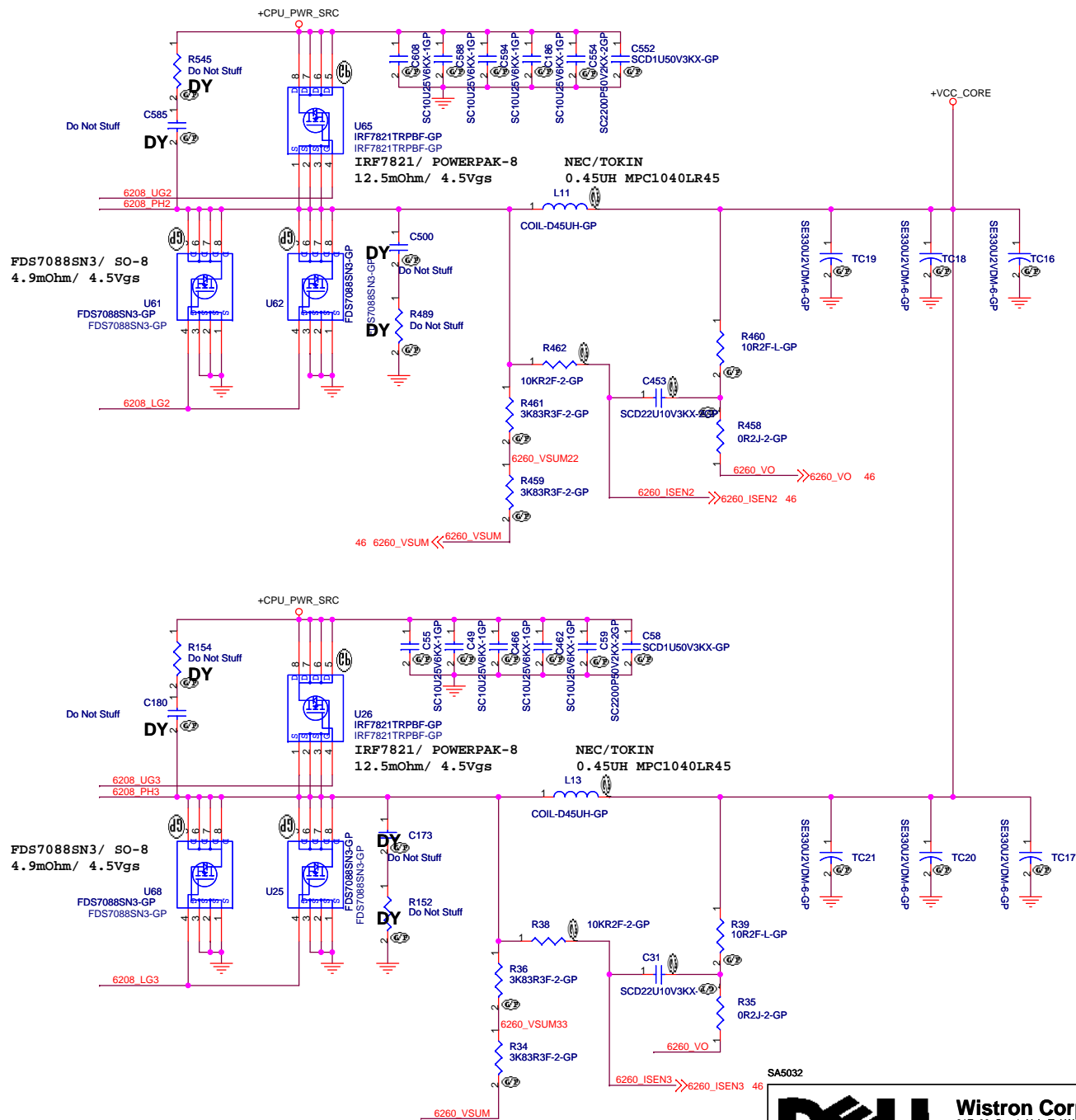
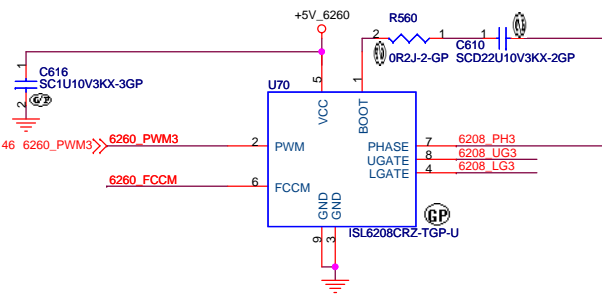
**DELL Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

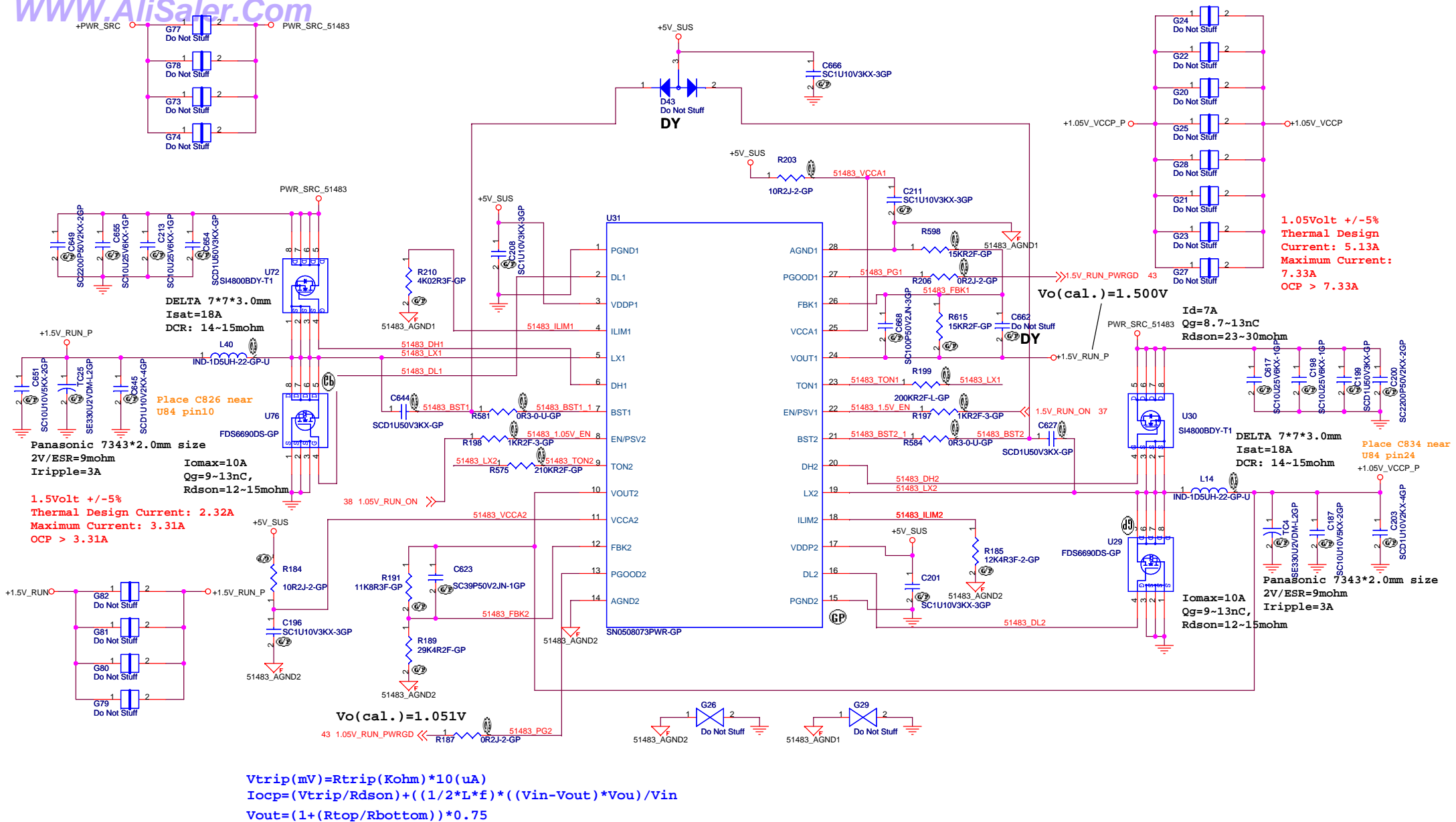
Title: **Charger**

Size: A3 Document Number: **Siberia / Converse** Rev: SA

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|  |       |
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|  | Title |
|--|-------|

### DC to DC 1.5V/ 1.05V

Size

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| Document Number |
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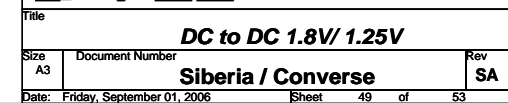
## Siberia / Converse

Date \_\_\_\_\_

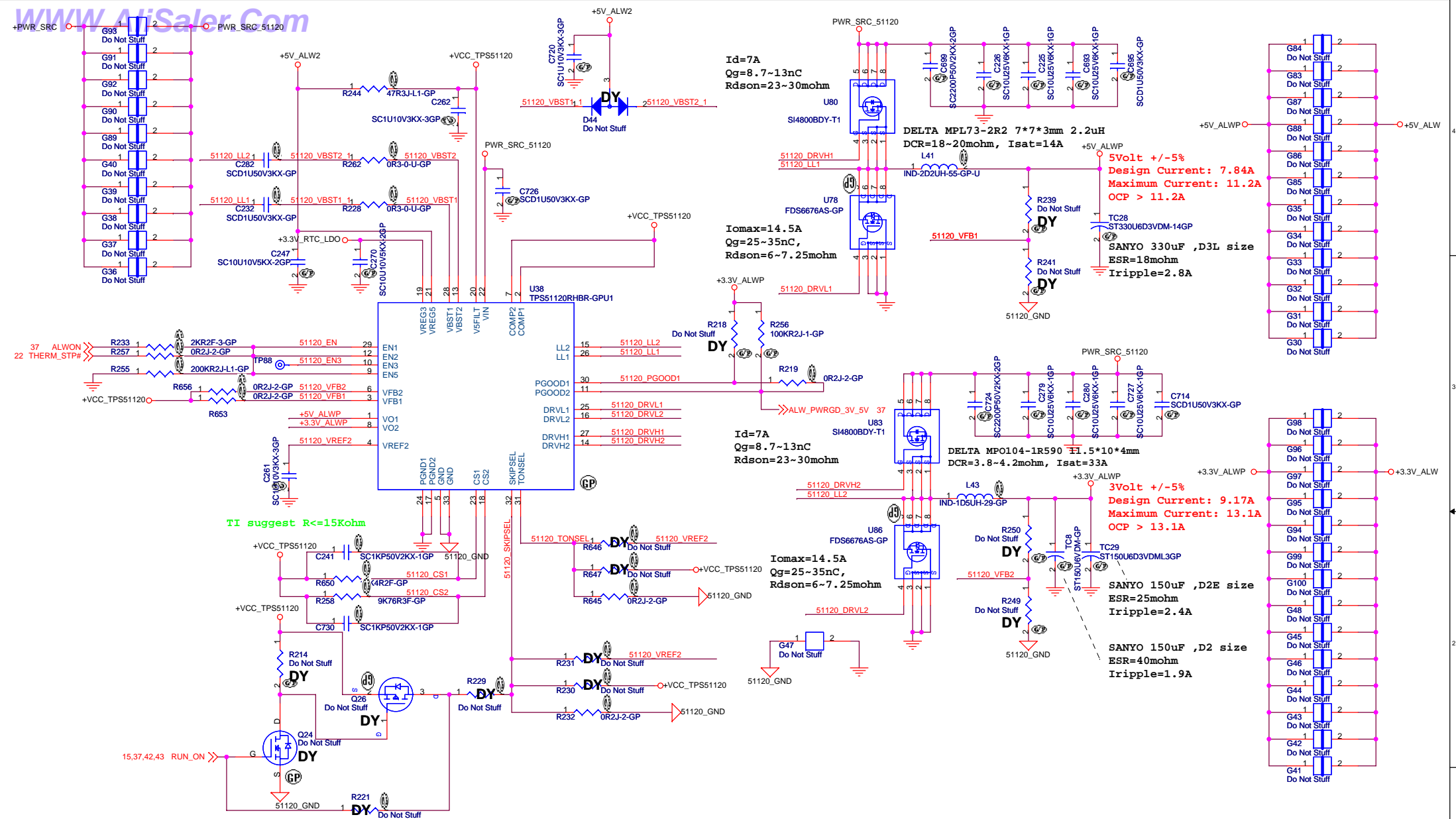
Friday, September 01, 2006

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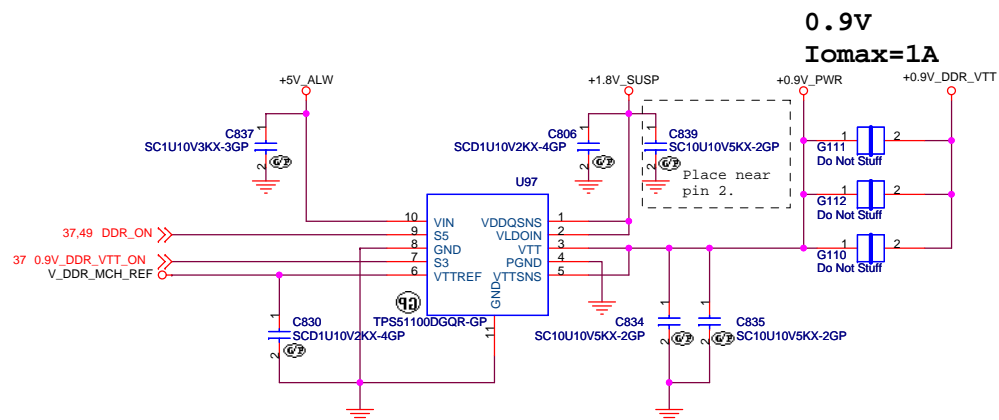
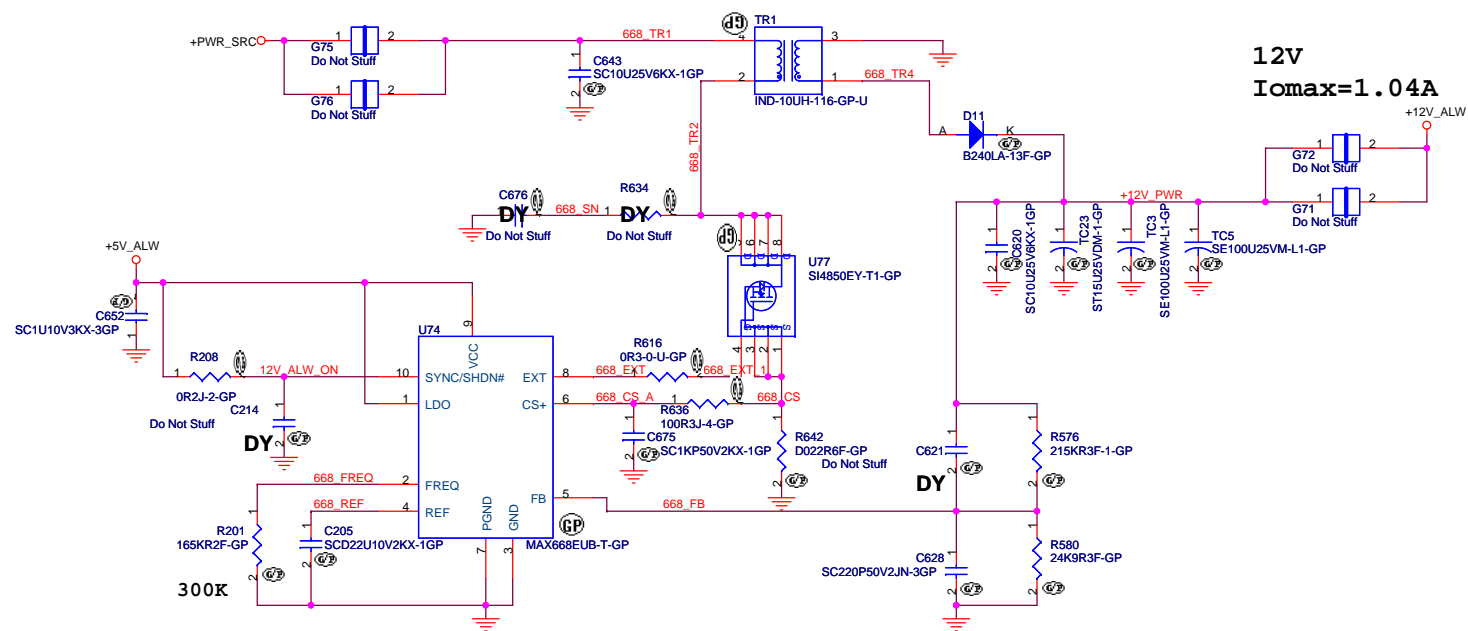






|         | ONG                  | VREF2                      | FLOAT                | VSFLT                 |
|---------|----------------------|----------------------------|----------------------|-----------------------|
| SKIPSEL | AUTOSKIP             | AUTOSKIP<br>/FAULTS<br>OFF | PWM                  | PWM                   |
| COMP    | N/A                  | N/A                        | CURRENT<br>MODE      | D-Cap<br>MODE         |
| TONSEL  | 380k/CH1<br>580k/CH2 | 280k/CH1<br>430k/CH2       | 220k/CH1<br>330k/CH2 | 180k/CH1<br>2870k/CH2 |
| VFB1    | N/A                  | not use                    | ADJ.                 | 5V<br>Fixed Output    |
| VFB2    | N/A                  | not use                    | ADJ.                 | 3.3V<br>Fixed Output  |
| EN1,EN2 | Switcher OFF         | not use                    | Switchchr ON         | Switcher ON           |
| EN3,EN5 | LDO OFF              | not use                    | LDO ON               | VREG3 ON              |

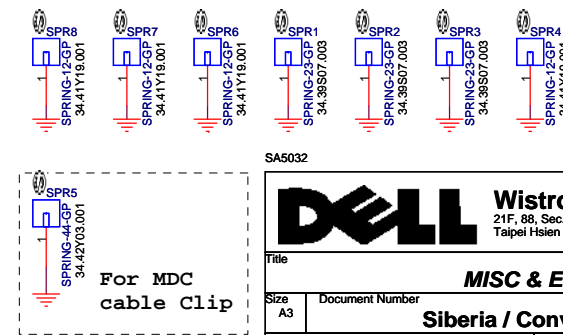
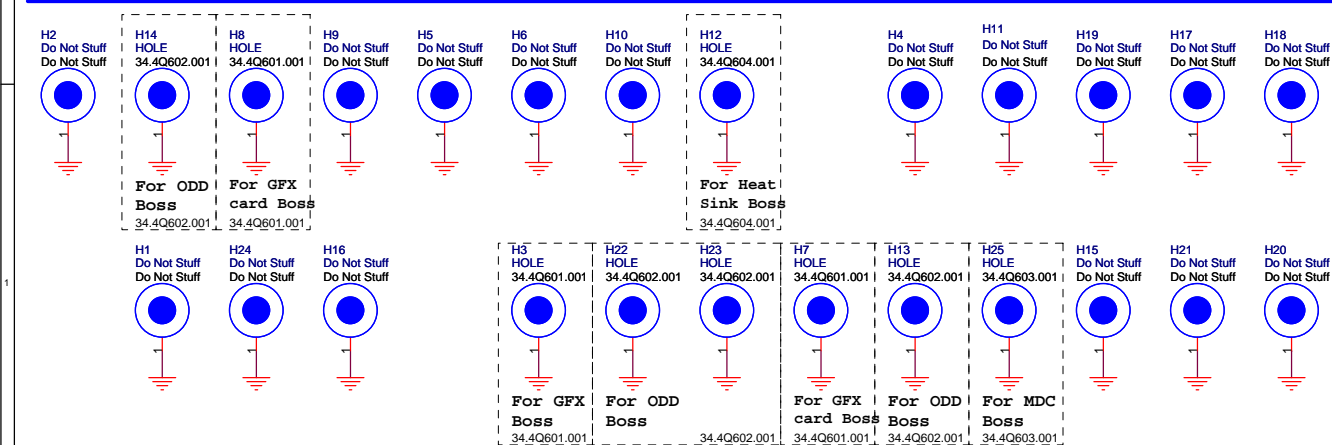
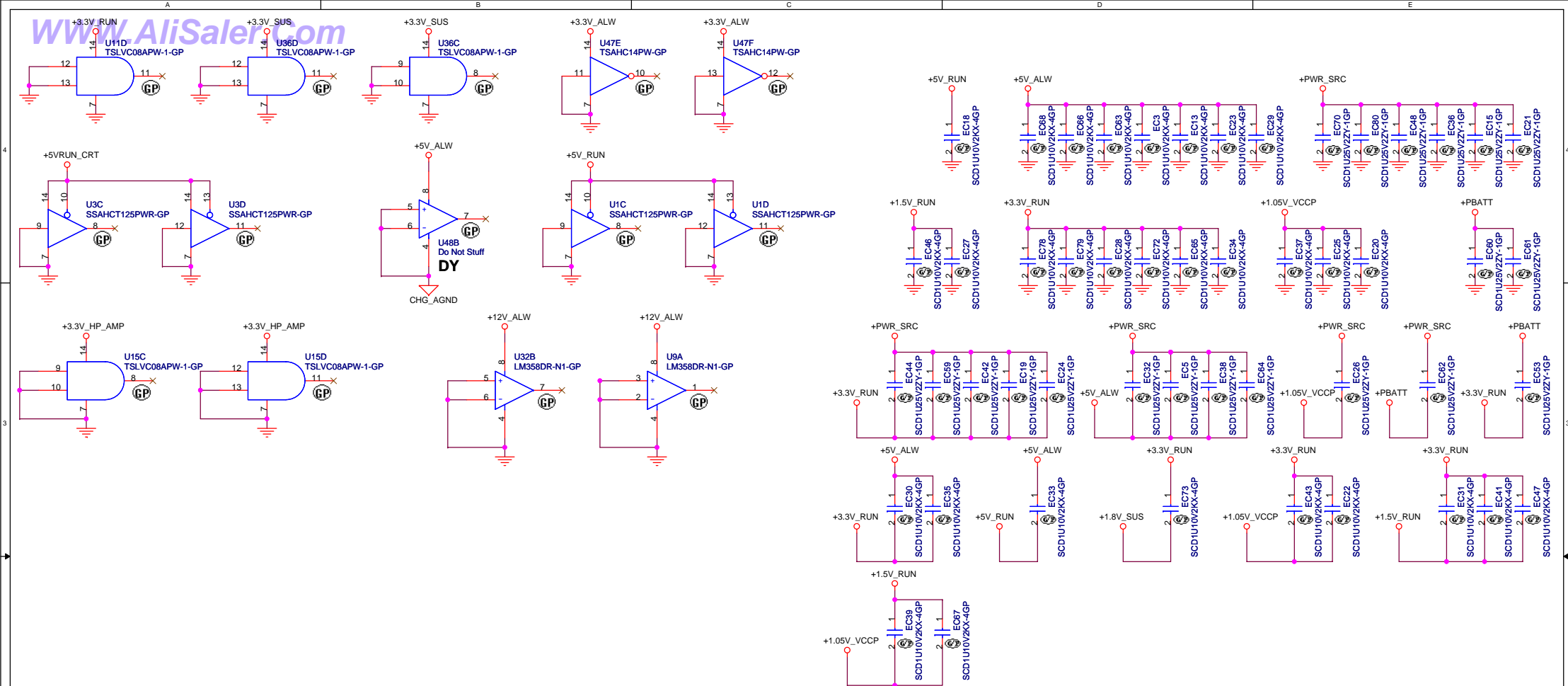
$$V_{out} = 1V * (R1 + R2) / R2$$



SA5032



|                     |                            |                |
|---------------------|----------------------------|----------------|
| Title               |                            |                |
| DC to DC 12V / 0.9V |                            |                |
| Size                | Document Number            | Rev            |
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| Date:               | Friday, September 01, 2006 | Sheet 51 of 53 |



SA5032



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**MISC & EMI**

Size

| Document Number |
|-----------------|
|-----------------|

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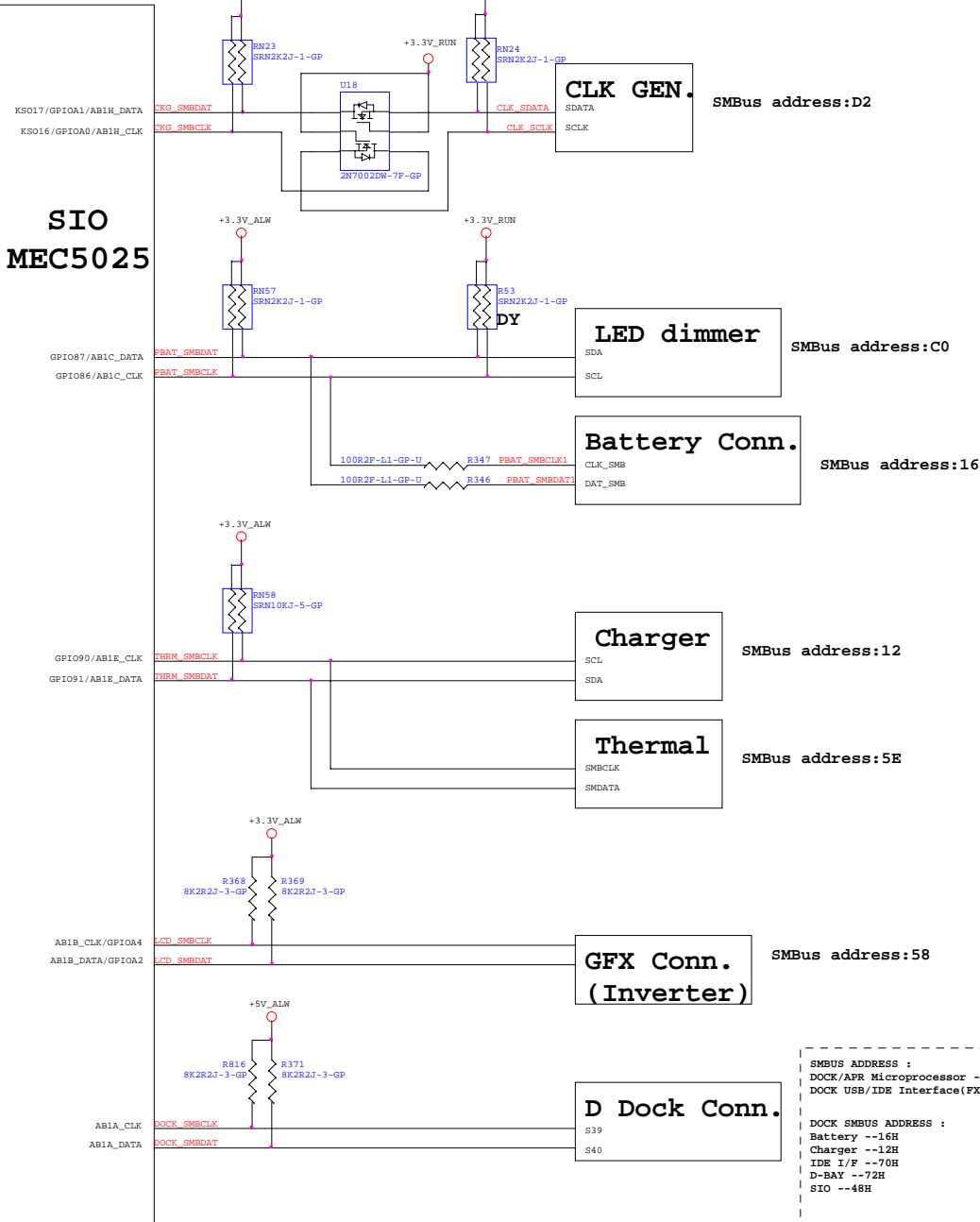
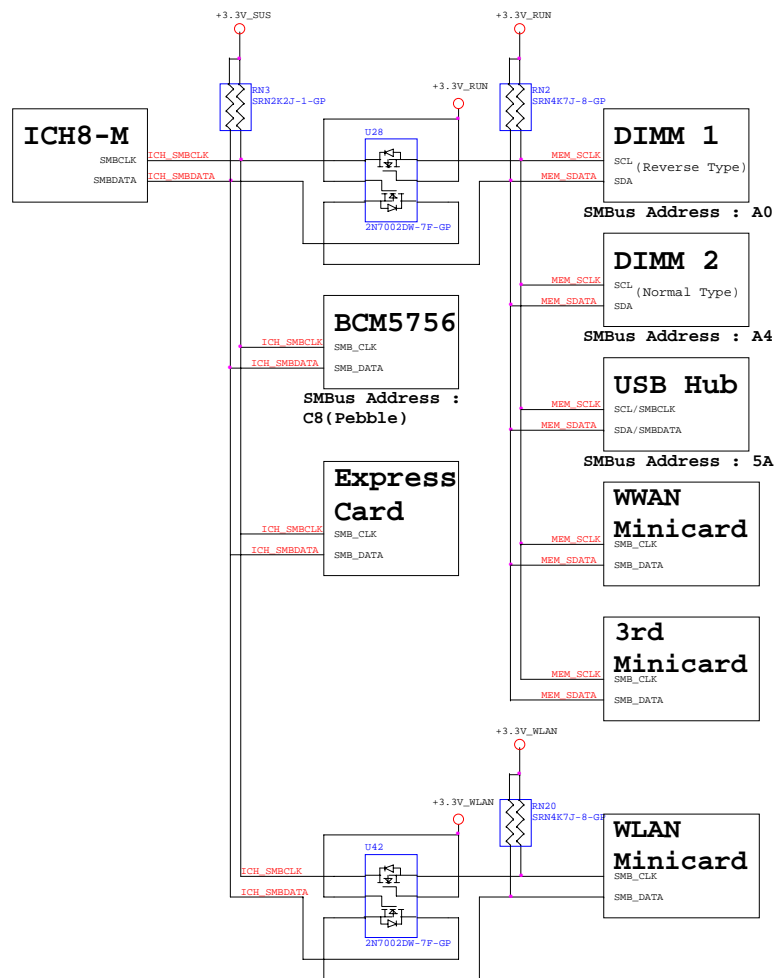
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Rev

# ICH8 SMBus Block Diagram

# KBC SMBus Block Diagram



SMBUS ADDRESS :

DOCK/APR Microprocessor --74H

DOCK USB/IDE Interface (FX2) --72H

DOCK SMBUS ADDRESS :

Battery --16H

Charger --12H

IDE I/F --70H

D-BAY --72H

SIO --48H